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Construction of *a* fault tree for Physical mixed Systems using logical gates associated with algebraic expression of top event via Boolean algebra rules to determine minimal cut sets for the system

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Abstract

The evaluation of a fault tree proceeds in two steps, the first is a logical expression for top events in terms of combinations of the basic event, the second this expression is used to give the probability of the top event in terms of the probabilities of the basic events. Boolean algebra rules are used in the two steps a hone which allows to simplify the logical expression , i.e., reducing the fault tree. Minimal cut sets from fault tree and path sets from sets dual (success tree) is introduce directly also.

Key Words:- FT Fault Trees , ST Sacess Trees , T Top Events

Some definitions and concepts:

Definition(1) : Fault Tree

A fault tree (FT) is a diagrammatic representation of all possible fault events , their logical combinations, and their relationship to the system failure[3].

Definition(2) : Basic Event

A basic event is a basic initiating fault event that requires no further development. It is symbolized by circle[4].

Definition(3) : Intermediate Event

An Intermediate Event is a fault event which occurs because of one or more antecedent causes acting through logic gates. All intermediate events are symbolized by rectangles[3, 6].

Definition(4) : A path Set

A path set is an event or combination of events whose non occurrence ensures the non occurrence of the top – level event. [5].

Definition(5) : A success tree(ST)

Is complements or dual of the fault tree and focuses on what's must happen for the top level event to be a success . [6].

The faults at the lowest level of the system are normally represented at the bottom of the tree and the system fault at the top.

The failure probabilities of basic events are combined to obtain the failure probabilities of intermediate events and finally the top event i.e., the system failure.

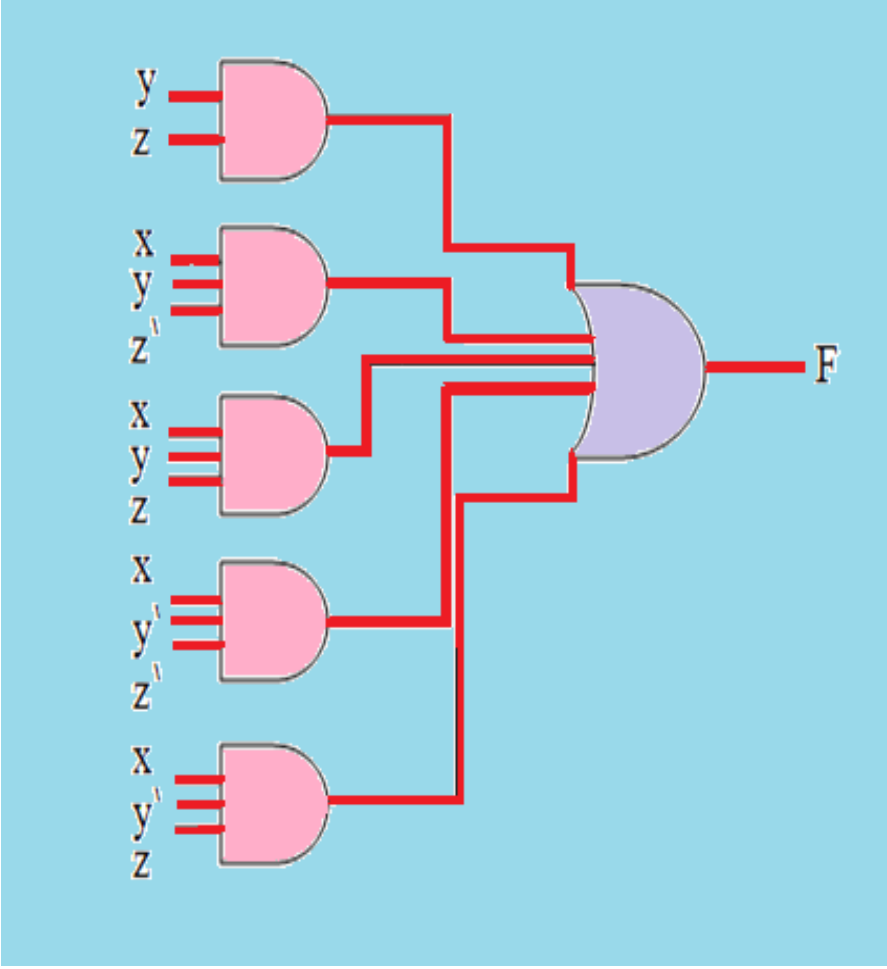
To develop a fault tree system , we must understand in detail how the system operates and what faults could possibly occur.

For this aim, flow graphs and system logic diagrams are usually used to show the relationship of all the components and events of states of the system. See[6].

We must identify interacting events which in turn produce other events by the use of simple logical relationships. The algebra of events i.e. Boolean algebra is applied in FT. For more details. See [3], [6]

Some illustrative Examples [1,2,5]**:**

Ex(1):- For the following algebraic expression the corresponding logical circuit is as shown in figure below (1):



Fig(1) The Corresponding Logical Current for Equation (1)

F= y z + x y z' + x y z + x y' z' + x y' z.....(1)

We can reduce equation (1) by using Boolean rules as follows:-

= y z + x(y z' + y z + y' z' + y' z)

= y z + x(y(z + z') + y'(z' + z))

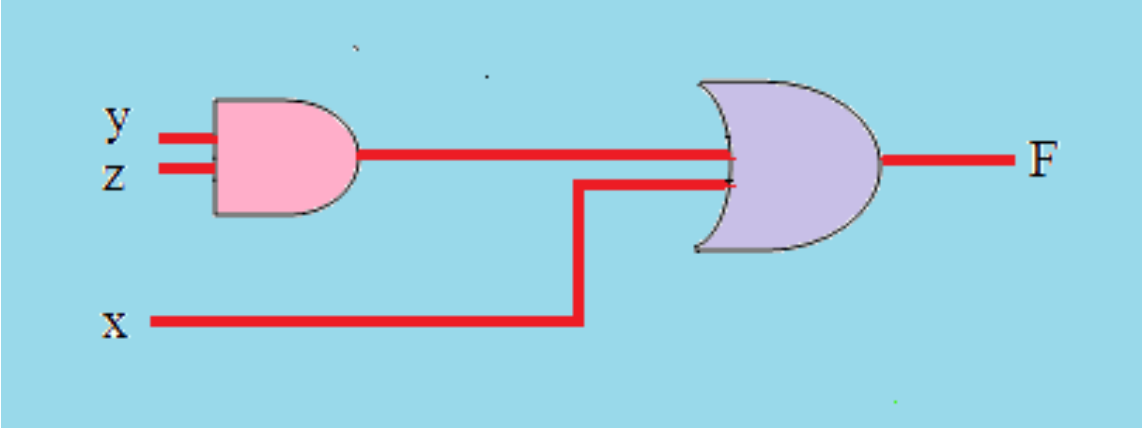
= y z + x(y(1) + y'(1))

= y z + x(y + y\)

= y z +x(1)

= y z +x ……..(2)

and the reduced logical circuit is as shown in figure bellow (2):



Fig(2) reduced logical circuit.

Ex(2):-

Consider a 3- component system as shown in Figure below (3)

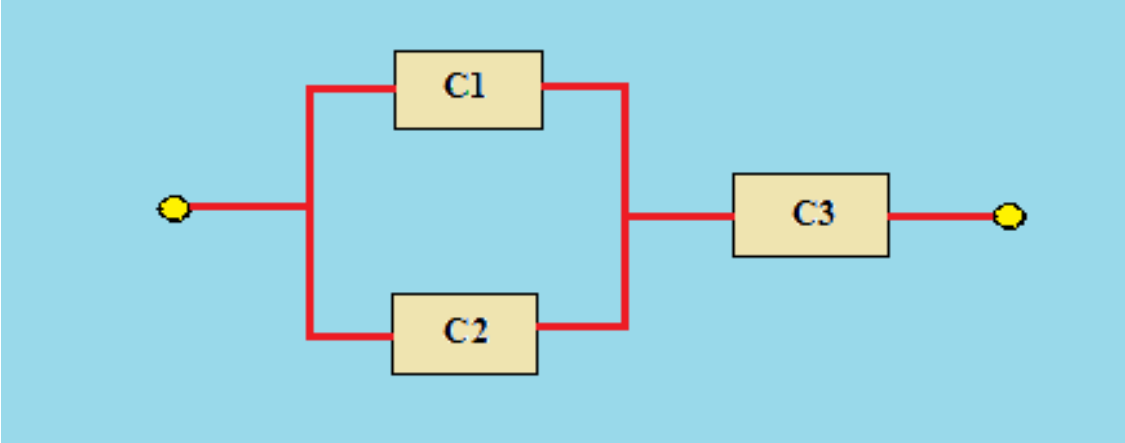


Fig. (3) A system consist of 3 components .

This system fails when the component C3 fails or both the components C1 and C2 fails , or all three components fails , the fault tree FT of the system is as shown in the following Figure by using the logical **AND** and **OR** gates**.**

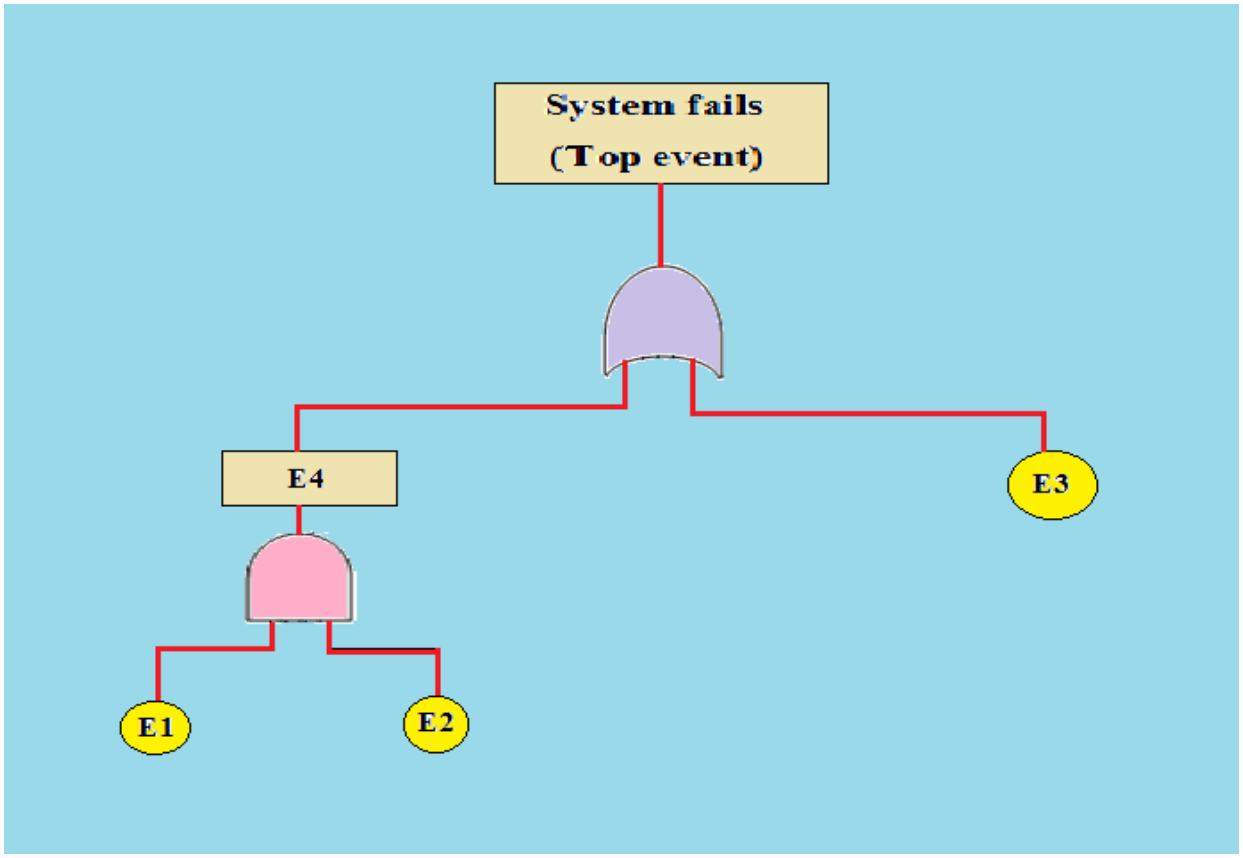


Fig (4) Fault tree for the system in Fig. (3)

Ex(3):- The Following physical system which consists of 8 components is shown in figure below(5) :-

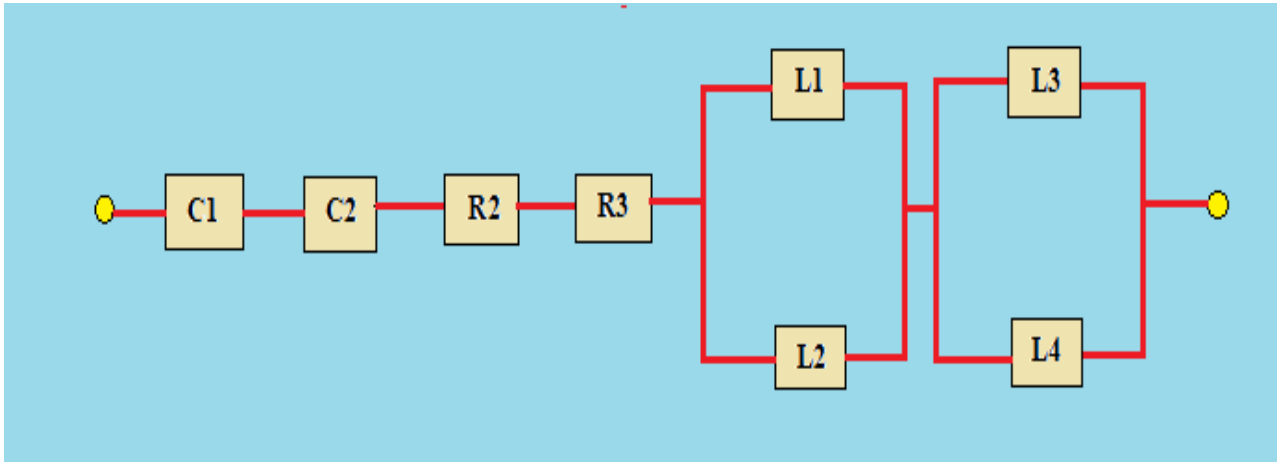


Fig.(5)A system consist of 8 components.

Ex(3):- Aboard circuit of motors control consists of eight components which are connected as shown in the following Figure. (6).

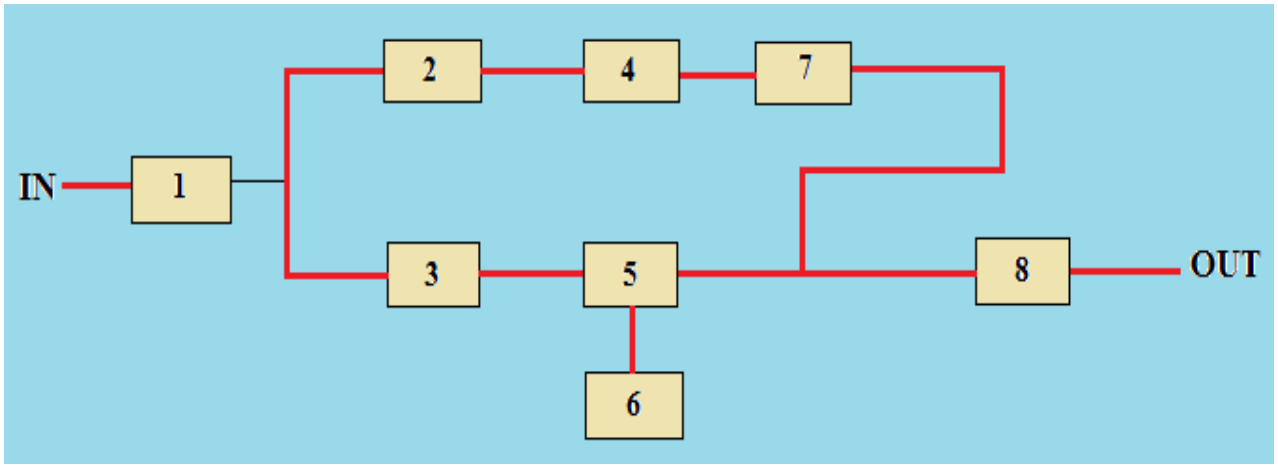


Fig. (6) Complex system

The network representation of the complex system above is as shown in figure below (7) .

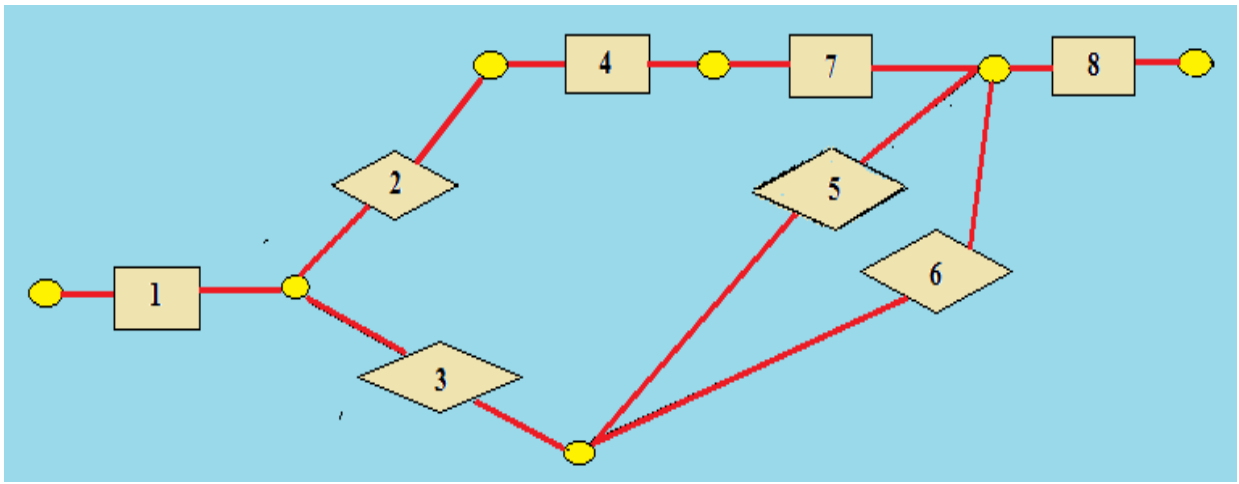


Fig. (7) Network representation of system in Fig. (6)

The system failure i.e., " Top event T "

$$T = A_1 + (A_2 + A_4 + A_7) \cdot (A_3 + A_5 \cdot A_6) + A_8 \quad \text{.....(3)}$$

Let $A_9 = A_{10} \cdot A_{11}$, $A_{10} = A_2 + A_4 + A_7$

$A_{11} = A_3 + A_5 \cdot A_6$, $A_{12} = A_5 \cdot A_6$

Which represent intermediate events.

$$T = A_1 + A_8 + A_2 A_3 + A_3 A_4 + A_3 A_7 + A_2 A_5 A_6 + A_4 A_5 A_6 + A_5 A_6 A_7 \text{ .....(4)}$$

Where the terms in the right of Equation (4) represent the cut sets of the top event . The following figure shows the FT of the system in example (4).

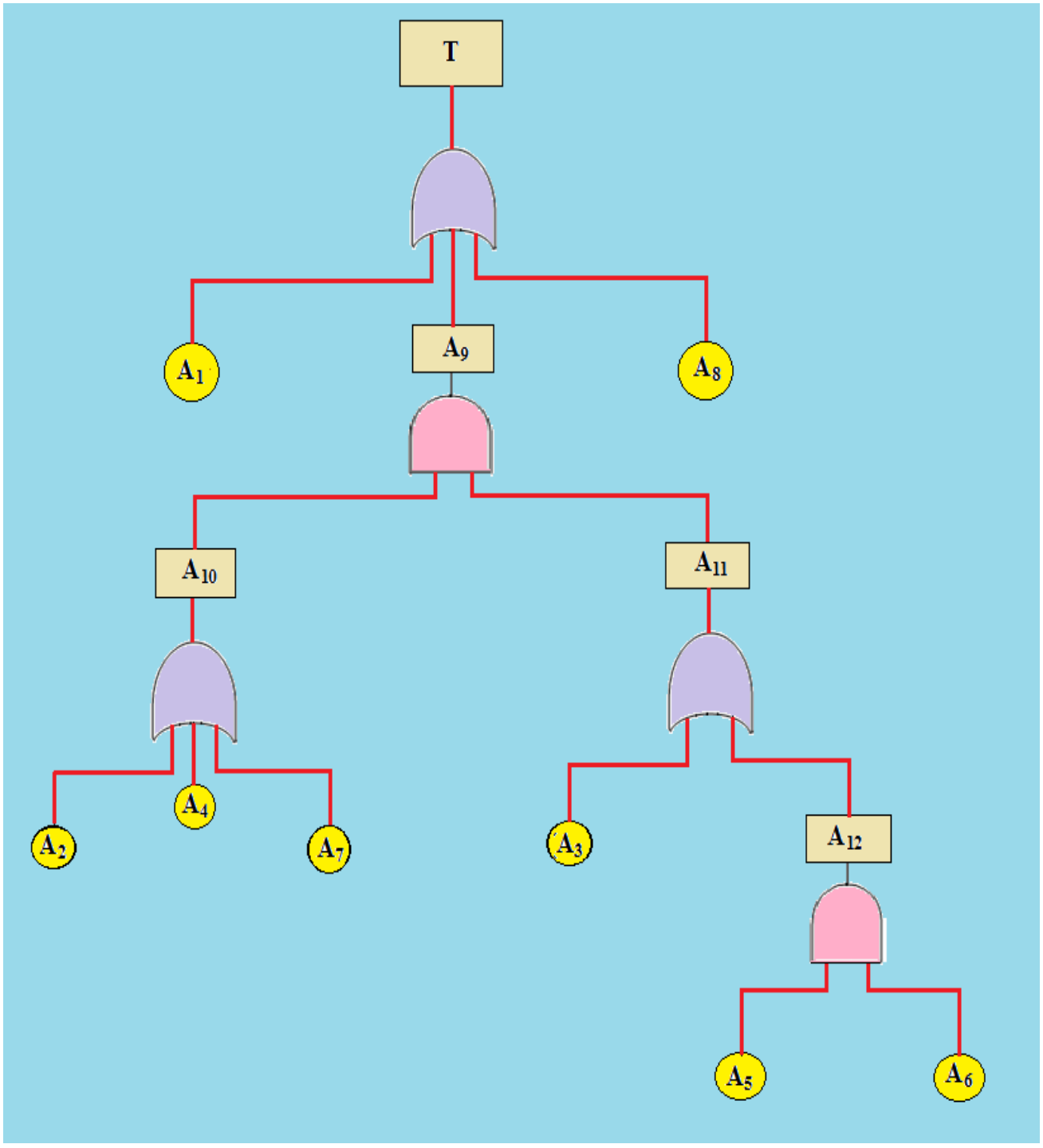


Fig. (8) F T of the system in example (3)

Now, to find the dual of FT , i.e., the success tree ST , we take the complement of the top event T in equation (4) as follows :

$$T^{\backslash} = A_1 \, . \, A_8 \, [\, (A_2 \, A_4 \, A_7 \,) + A_3 \, . \, (A_5 + A_6 \,) \,]$$

$$= A_1 \, A_8 \, A_2 \, A_4 \, A_7 + A_1 \, A_3 \, A_5 \, A_8 + A_1 \, A_3 \, A_6 \, A_8 \qquad \text{…….(5)}$$

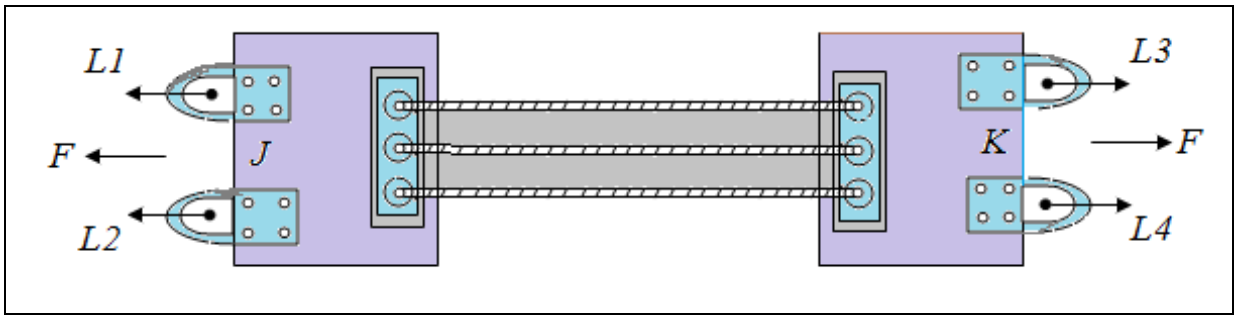
Where the right side of the equation (5) represents the path sets R_1 , R_2 and R_3.

Ex(4): figure **(9)** shows a device designed to haul heavy weights. Three steel ropes are connected to two heavy end plates J and K. Each end plate has two U-links bolted to it and each U-link is held by four bolts. When the applied load exceeds the design load, failure of the device may occur due to one or more of the following causes:

(a) Failure of the bolts holding each U-link. Since there are four bolts holding each link, the failure of each of these bolts may be denoted by B1, B2, B3, B4.

(b) Any two of the steel ropes, or all the three ropes may fail due to overstressing. Let R2 denote the failure of two ropes and R3 the failure of all the three ropes.

(c) The fixtures of the ropes to each of the due plates may fail. Denote these by C1 and C2 referring to the left and right end plate fixtures, respectively.



Fig(9)

The fault tree for the failer of the above device as shown in follwing fiqure(10):

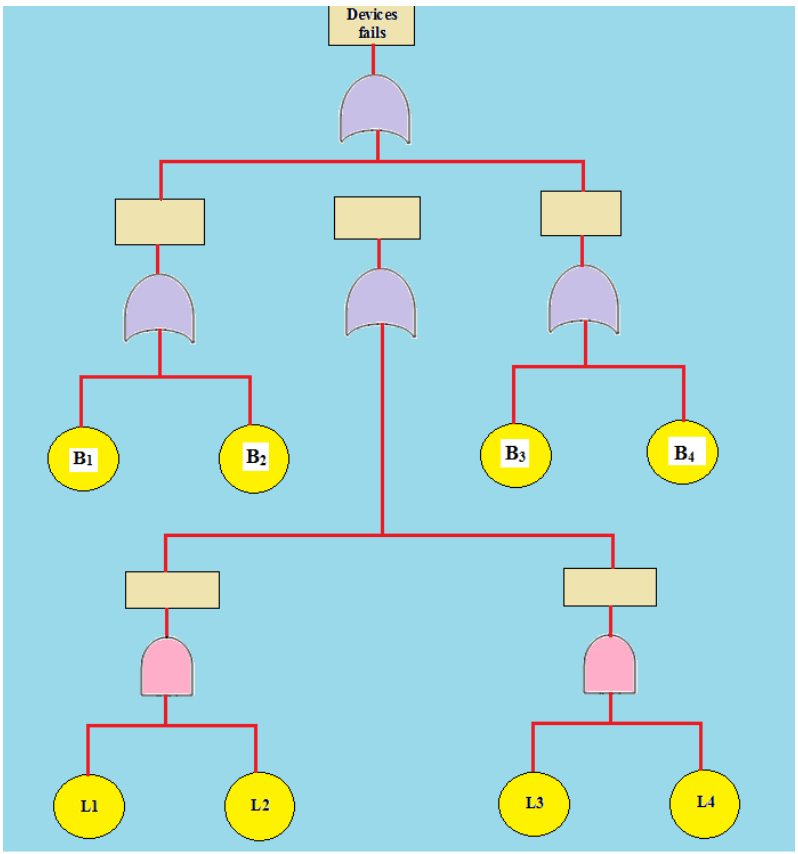


FIG.(10)

Conclusions:

1. The use of logical gates is very useful to convert the algebraic expression into the corresponding logical circuit or fault tree and vice versa.

2. An " **OR** " gate always increase the number of cut sets there will be a separate cut set for every OR gate input.

3. An " **AND** " gate always increase the size of a cut sets. (there will be one a cut set for an AND each input increase the size of cut sets.

4. The suggested method can be used to obtain cut sets directly from fault a given fault tree and alese path sets by using the taking the complements for the algebraic expression the corresponding (success tree (ST) or dual tree simplify (reducing) the bolean algebraic expression (by using the laws of bolean algebra).

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