Journal of Information Engineering and Applications
ISSN 2224-5782 (print) ISSN 2225-0506 (online)
Vol 2, No.3, 2012

A comparative study of Total Harmonic Distortion in Multi level inverter topologies

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Abstract

This paper presents a detailed harmonic analysis in terms of Total Harmonic Distortion (THD) for different power circuit topologies of multi level inverter fed induction motor drives. The most common multilevel inverter topologies are the neutral-point-clamped inverter (NPC), flying capacitor inverter (FC), and cascaded H-bridge inverter (CHB). This work is to analyze the performance of all the power circuit topologies of multilevel inverter with various multi carrier PWM control techniques. Simulation and results shows that the superiority of these inverters over two-level pulse width modulation based inverter fed drives.

Keywords: Medium-voltage drives, Multi Carrier PWM, Multi level inverter, Induction motor drives.

1. INTRODUCTION

Present day drive types are the Induction motor drives with voltage source inverters. Also the voltage waveforms of traditional two level inverter fed Induction motor shows that the voltage across the motor contains not only the required "fundamental" sinusoidal components, but also pulses of voltage i.e. "ripple" voltage. Moreover the voltage waveforms produced by the inverter has sharp edges. The rate of change of voltage with respect to time i.e. dv/dt is very high at these edges, of the order of 500–5000 V/μs. Although high voltage ratings of the power semiconductor devices are available, it is Inadvisable to retain the 2-level configuration for higher voltage motors. This is because high voltage pulses will be applied to the motor causing dv/dt stresses. Today, medium voltage induction motors rated at the MW level are generally controlled using three level inverters. The 3-Level inverter, on the other hand, allows the motor voltage to go up in steps. This reduces the dv/dt stress for the same DC bus voltage V_{dc}. Inverters of higher number of levels such as 5 and 7 level can also be constructed. However, the circuit assembly becomes very complex and issues such as keeping all the sections of the dc bus voltage equal have to be addressed [1]. The general structure of the multilevel converter is to synthesize a sinusoidal voltage from several levels of voltages, typically obtained from capacitor voltage sources. As the number of levels increases, the synthesized output waveform adds more steps, producing a staircase wave which approaches the sinusoidal wave with minimum harmonic distortion. The stepped waveform is synthesized by selecting different voltage levels generated by the proper connection of the load to the different capacitive voltage sources. This connection is performed by the proper switching of the power semiconductors.

1.1 The general structure

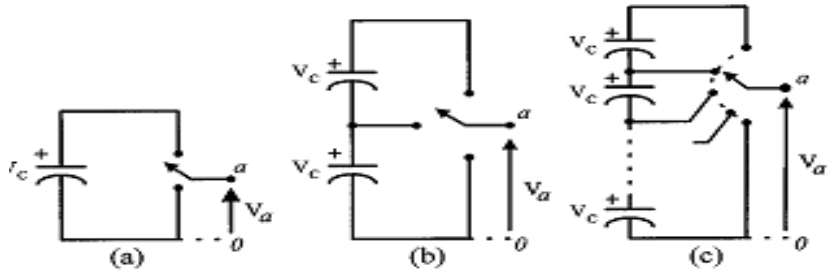

Figure 1. One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels

In Figure 1(a) the output V_a can take two possible values i.e. 0 and V_c . In Figure 1(b) the output V_a can take three possible values i.e. 0,V_c and $2V_c$. In Figure 1(c) the output V_a can take four possible values i.e . 0,V_c , $2V_c$ and $3V_c$. It can be extended further. The number of possible outputs represents the level of the inverter that is shown in Figure 1(d).

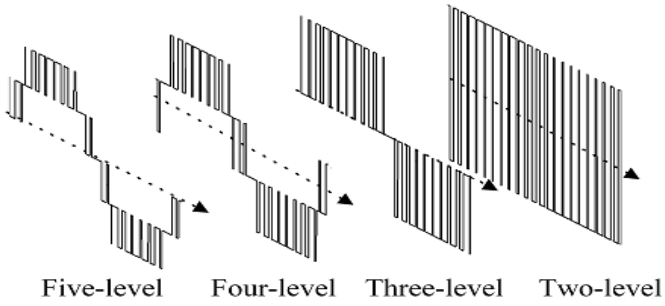

Figure 1.(d) Output voltage levels of an inverter

When considering a three-phase system, the levels of one phase are combined with those of the other phases, generating more different levels in the line-to-line voltage.For a converter with n_p phase to neutral voltage levels, $n_{ll}=2n_p-1$ levels can be found in the line-to-line voltage (a zero level is redundant) [2].

2. GENERAL TOPOLOGIES OF MULTI LEVEL INVERTER

2.1 Neutral point clamped inverter (NPC)

The neutral point clamped topology is also known as diode clamped topology. The main advantage of the NPC topology is that it requires only one DC source similar to two- level inverter, and gives better performance. With the increase in level ‘n’, not only the number of clamping diodes increases but also the problem of ensuring the DC-link balance becomes more severe. Due to these reasons, the NPC topology is mainly used for 3- level inverter. Figure 2 shows its 3-level NPC topology.

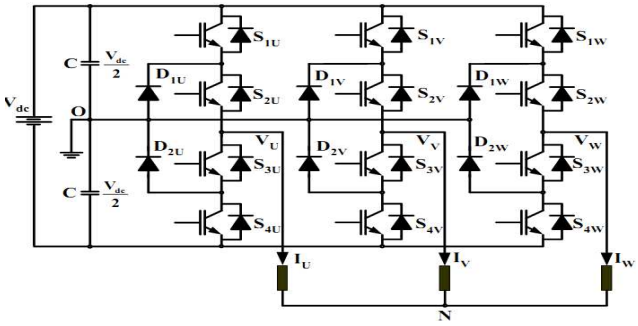

Figure 2. Three -level Neutral Point Clamped topology

2.2 Flying Capacitor Topology (FC)

It is also known as capacitor clamped topology. For this topology 'n' can take any integer value similar to NPC topology. The voltage clamping is done by using capacitors floating with respect to the earth potential. Figure 3 shows its 3-level topology. However, this topology also exhibits the capacitor voltage unbalancing problem.

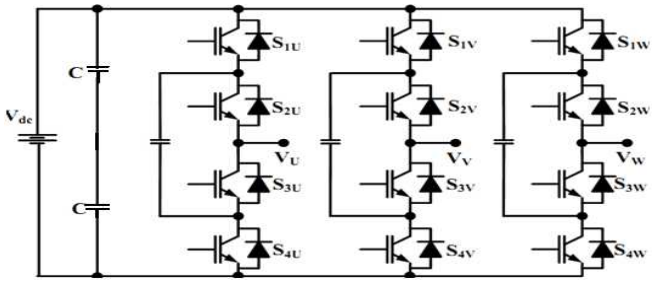

Figure 3. Three-level Flying Capacitor topology

Since this topology offers more redundancy as compared to NPC topology, the capacitor voltage unbalancing can be reduced by utilizing these redundancies. The main disadvantage of this topology is that it needs a large number of bulky capacitors that inhibits the industrial use of this topology.

2.3 Cascaded H-bridge Topology (CHB)

In this topology the H-bridges are cascaded in every phase. With the increase in H- bridges in a phase, the output voltage waveform tends to be more sinusoidal. Figure 4 shows its 5-level topology. It consists of two identical H-bridges in each phase. In n-level topology, (n-1)/2 identical H- Bridges are used in every phase. There must be a separate DC source for the DC bus of every individual H-bridge. Hence, this topology is useful for collecting energy from renewable energy resources e.g. solar panels and fuel cell.

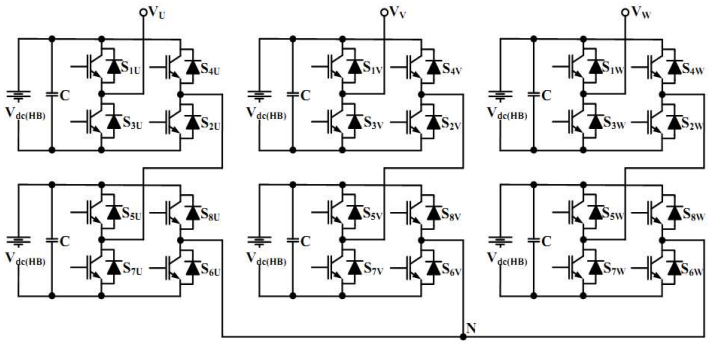

Figure 4. Five-level Cascaded H-Bridge Topology

1. Multi level inverter modulation control schemes

Figure 5 shows the multilevel converter modulation methods. The modulation control schemes for the multilevel inverter can be divided into two categories, fundamental switching frequency and high switching frequency PWM such as multilevel carrier-based PWM, selective harmonic elimination and multilevel space vector PWM Multilevel SPWM needs multiple carriers. Each DC source needs its own carrier. Several multi-carrier techniques have been developed to reduce the distortion in multilevel converters, based on the conventional SPWM with triangular carriers. Some methods use carrier disposition and others use phase shifting of multiple carrier signals. By generalizing, for an 'n' level multilevel inverter, (n-1) carriers are needed. The implementation of the various carrier PWM techniques that is possible for multi-level inverters are [3]-[6]:

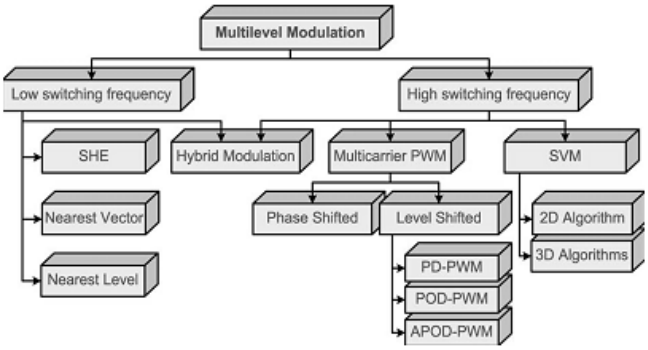

Figure 5. Multilevel converter modulation methods

3.1 Level Shifted PWM (LSPWM)

This modulation method is especially useful for NPC converters, since each carrier can be easily associated to two power switches of the converter. LSPWM leads to less distorted line voltages since all the carriers are in phase compared to PSPWM [8]. In addition, since it is based on the output voltage levels of an inverter, this principle can be adapted to any multilevel converter topology. However, this method is not

preferred for CHB and FC, since it causes an uneven power distribution among the different cells. This generates input current distortion in the CHB and capacitor unbalance in the FC compared to PSPWM [3]-[6]. Figure 6 shows the LS-PWM carrier arrangements.

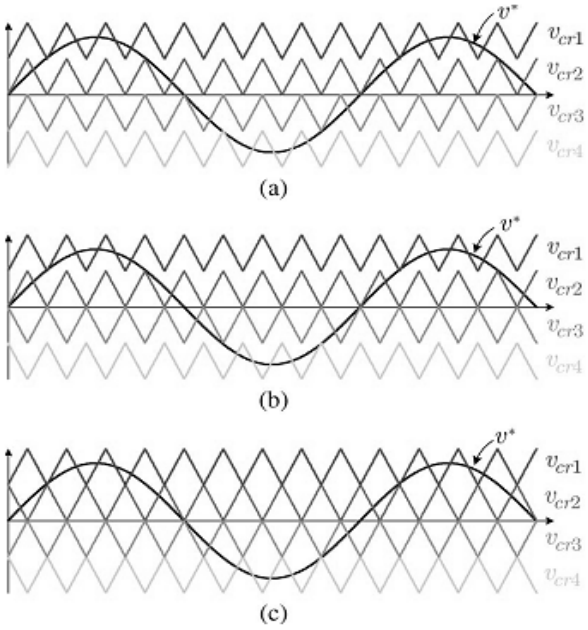

Figure 6. LS-PWM carrier arrangements: (a) PD, (b) POD, and (c) APOD.

3.1.1 Alternative phase opposition disposition (APOD) technique:

This technique requires f our carrier waveforms, which are phase-displaced by 180^o alternately.

3.1.2 Phase opposition disposition (POD) technique:

This technique requires four carrier waveforms that are all in phase above or below the zero reference value. However, they are phase shifted by180^o between the carrier waveforms above and below zero.

3.1.3 Phase disposition (PD) technique:

With the wide application in multi -level inverters, this technique has all carriers in phase. It requires four carrier waveforms. The zero reference is placed in the middle of the carrier sets.

3.2 Phase shifted PWM (PSPWM)

This technique uses a set of carriers that are all phase-shifted. The four triangular carriers are phase-shifted by 90^o. Using the same sampling period, it has four times larger switching frequency than that of other techniques. This technique is specially conceived for FC and CHB converters. Since each FC cell is a two-level converter, and each CHB cell is a three-level inverter, the traditional bipolar and unipolar PWM techniques can be used, respectively. Due to the modularity of these topologies, each cell can be modulated independently using the same reference signal. A phase shift is introduced between the carrier signals of contiguous cells, producing a phase-shifted switching pattern between them. In this way, when connected

together, a stepped multilevel waveform is originated. It has been demonstrated that the lowest distortion can be achieved when the phase shifts between carriers are 180^o or $360^o/k$ for a CHB or FC converter, respectively (where 'k' is the number of power cells). This difference is related to the fact that the FC and CHB cells generate two and three levels, respectively.

3.3 CONTROL DIAGRAMS

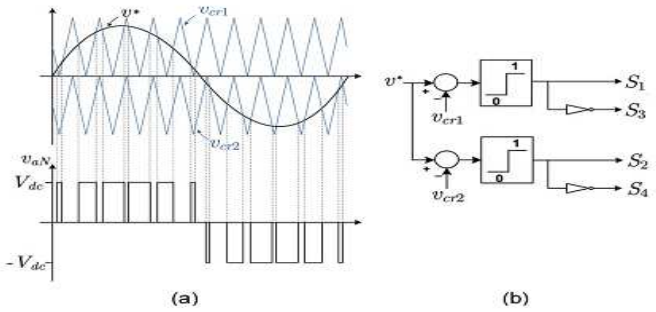

Figure 7. LSPWM for NPC: (a) waveform generation (b) control diagram.

From the Figure 7(a) and 7(b) it can be observed that the time, during which the value of the reference is greater than the value of both carriers, the upper switches are turned on connecting the load to the positive bus bar. During the times the reference value is between both carriers $V_{cr2} \leq V^* \leq V_{cr1}$, the output is connected to the neutral point N. Finally, the times in which the reference value is lower than both carriers, the lower switches are turned on, connecting the load to the negative bus bar.

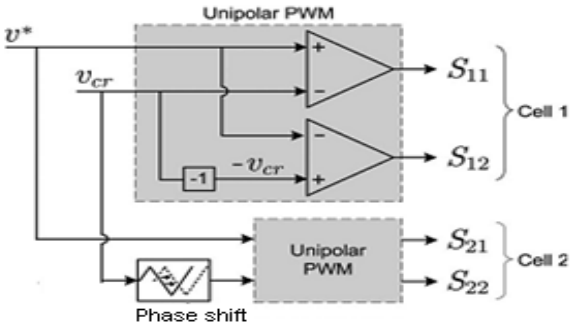

Figure 7(c). PS-PWM control diagram for CHB.

Here all the cells are controlled with the same reference and same carrier frequency with the required phase shift. The corresponding implementation diagram is illustrated in Figure 7(c).

2. Analysis of output line to line voltage Harmonics

In this section, simulation results using the proposed control techniques are presented. Simulation has been performed in Matlab/Simulink. To evaluate the inverter topologies for a variety of applications, carrier frequencies of f_c= 450Hz ..1050Hz are assumed for all investigated inverter topologies. This range is typical for available industrial medium voltage drives [11]. Also all the inverter topologies are connected to the Induction motor load. To validate the proposed method, the simulation of conventional two level PWM voltage source inverter (VSI) fed induction motor is performed and the outputs are obtained. Figure 8 shows the harmonics produced by two level VSI and it is recorded to be 38.68%. Also the seventh harmonic is dominant in this harmonic spectrum.

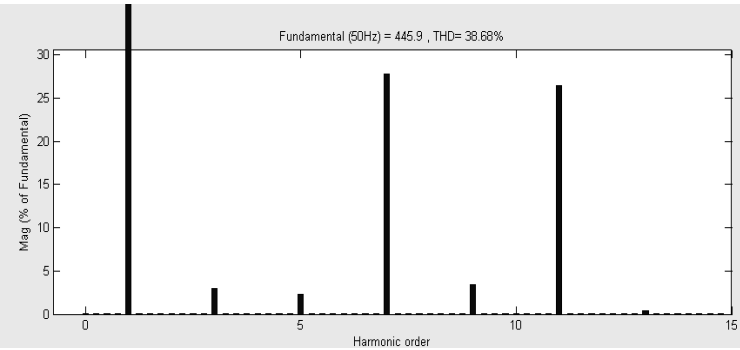

Figure 8. Harmonic spectrum of line voltage for Two level VSI

4.1 Neutral Point Clamped inverter

The neutral point clamped inverter with LC filter fed to the Induction motor load is controlled by means of two numbers of carriers with level shifted PWM. Basic control block diagram is shown in fig.7: (b). In this work an optimal value of modulation index of 0.8 and the switching frequency of 750HZ has been selected to get much better performance [11]. The minimum dc-link voltage to achieve an required output line-line voltage can be calculated by

$$V_{dc,min} = \sqrt{2} \times V_{LL,rms}$$

To determine the nominal dc-link voltage of the converter, a dc-link voltage reserve of 4% is required to cover the voltage drop across the filter [11].

$$V_{dc,n} = 1\,04 \times V_{dc,min}$$

Different criteria are given in the literature for the dimensioning of the dc link capacitor [11], in order to choose the most suitable amount and size of dc link capacitors. In this work 2.33mF has been selected to provide great reduction in DC link voltage ripple [11]. Figure 9 shows the Total Harmonic Distortion (THD) that will decrease significantly to 17.53% as compared to the conventional two level inverter from 38.68%. Also it was observed the seventh harmonic is absent in this spectrum.

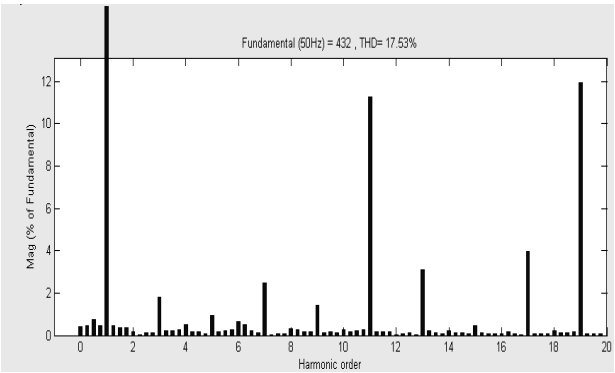

Figure 9. Harmonic spectrum of line voltage for NPC

4.2 Flying Capacitor inverter

Three level flying capacitor multi level inverter with LC filter fed to the Induction motor load is simulated. Figure 10 shows the harmonic spectrum for the output phase voltage of three level flying capacitor inverter. Here it is shown that 26.35% of harmonics present in the output line-line voltage. i.e The THD will decreases significantly to 26.35%. To get the maximum converter efficiency the switching frequency of 500HZ and the flying capacitors of 3344µF has been selected for this topology [11].

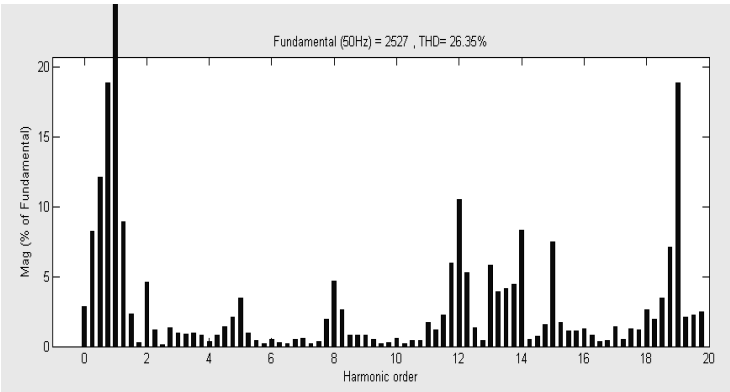

Figure 10. Harmonic spectrum of line voltage for FC

4.3 Three Phase Cascaded H-Bridge (CHB) inverter

It consists of two identical H-bridges in each phase [7]-[9]. PSPWM method of technique is used to control the inverter power devices. Basic control block diagram is shown in figure 7(c). It uses four numbers of carriers to get five level output phase voltage. The carriers are displaced by 90^{o} with each other.

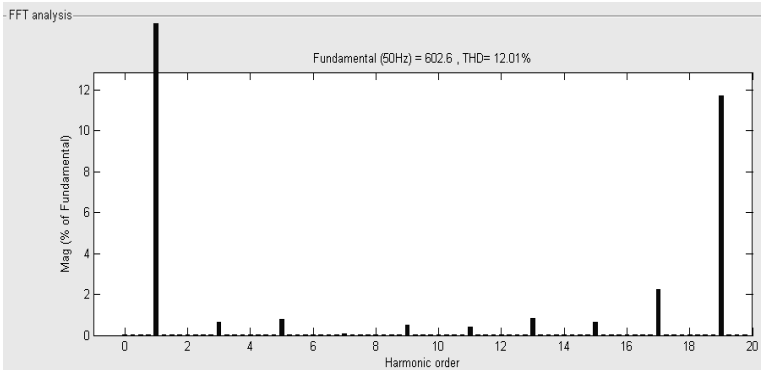

Figure 11. Harmonic spectrum of CHB inverter

The simulation of Cascaded H-bridge inverter yields harmonic spectrum as shown in Figure 11. Here it was shown that the THD is significantly reduces to 12.01%. Also the most of the lower order harmonics are suppressed.

4.4 Comparisons

Table.I. Comparison of THD

Power Circuit Topology	Vline-line THD (%)
Two level VSI	38.68
3 level FLC	26.35
3 level NPC	17.53
5 level CHB	12.01

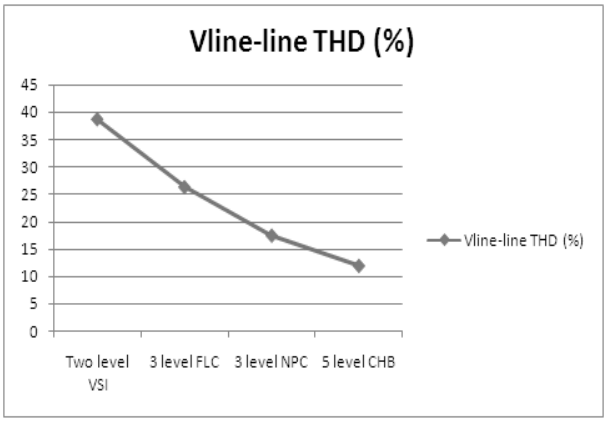

Figure12. Comparison of THD for all the investigated inverter topologies

The comparison in terms of THD is given in Table .I and the respective graph plot is given in Figure 12. These topologies have also been compared in terms of structure, cost, and efficiency. The voltage waveforms of traditional two level inverter fed Induction motor shows that the voltage across the motor contains not only the required "fundamental" sinusoidal components, but also pulses of voltage i.e. The harmonics are higher and obtained as 38.68%. Moreover the voltage waveforms produced by the inverter has sharp edges. Thus the high voltage pulses applied to the motor causing dv/dt stresses. In case of 3 level NPC the main drawbacks are the requirement of clamping diodes, the lack of modularity, and the unequal semiconductor-loss distribution. Furthermore, voltage-balancing problems and a reduced silicon utilization due to the increasing voltage-blocking stress of the clamping diodes are severe structural problems of diode-clamped converters with more than three levels. In contrast, the additional expense of flying capacitors, particularly at low carrier frequencies (e.g., fc < 800− 1000 Hz) and a high number of cells, are the main disadvantage of the FC topology. For the CHB, the main disadvantage is the separate dc sources, usually provided by a bulky and nonstandard transformer. On the other hand, the FC and CHB have modular structures, enabling a more natural implementation under fault operation, and design of power-electronics building blocks. The CHB is particularly necessary for very high-power applications since the series connection enables a natural increase of the power level of the converter. The FC has found its place in Medium Voltage traction drives. Finally, the NPC has experienced a substantial market penetration in 2.3–4.16-kV applications that require a low switching frequency and high converter efficiency at a lower cost as compared to the other two topologies.

3. Conclusion

This paper proposes the three multilevel topologies (3LNPC, 3L FC-VSI, and the 5-level CHB) and they cover different needs for different type of applications. The multi carrier PWM modulation control techniques are introduced in these topologies to get reduced harmonics at the output voltage THD and to improve the efficiency of the inverter. Thus the proposed inverter topologies with the proposed modulation method control techniques are validated through the detailed simulation analysis along with the conventional two level voltage source inverter, and it was shown that the output voltage levels are increased in the multi level inverters to approach near sine wave and to get the higher voltage and reduced Total Harmonic Distortion.

ACKNOWLEDGEMENTS

The authors thank the Management, the Principal & EEE Department of Thiagarajar College of Engineering for providing the necessary facilities to carry out this work.

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