Innovative Systems Design and Engineering
ISSN 2222-1727 (Paper) ISSN 2222-2871 (Online)
Vol.7, No.9, 2016

Modified SVPWM Algorithm for 3-Level Inverter Fed DTC Induction Motor Drive

B.Pradeep kumar reddy
M.Tech student EEE dept., RGMCET,Nandyal,A.P.

G.Kumaraswamy
Assoc.professor in EEE dept., RGMCET,Nandyal,A.P.

K. Sri Gowri
Professor in EEE dept., RGMCET,Nandyal,A.P.

Abstract
In this paper, a modified space vector pulse width modulation (MSVPWM) algorithm is developed for 3-level inverter fed direct torque controlled induction motor drive (DTC-IMD). MSVPWM algorithm simplifies conventional space vector pulse width modulation (CSVPWM) algorithm for multilevel inverter(MLI), whose complexity lies in sector/subsector/sub-subsector identification; which will commensurate with number of levels. In the proposed algorithm sectors are identified as in two level inverter and subsectors/sub-subsectors are identified by shifting the original reference vector to sector 1 (S1). This is valid due to the fact that a three level space vector plane is a composition of six two level space planes, and are symmetrical with reference to six pivot states. Switching state/sequence selection is also very important while dealing with SVPWM strategy for MLI. In the proposed algorithm out of 27 available switching states apt switching state is selected based on sector and subsector number, such that voltage ripple is considerably less. To validate the proposed algorithm, it is tested on a three level neutral point clamped (NPC) inverter fed DTC-IMD. The performance of the MSVPWM algorithm is analyzed by comparing no load stator current ripple of the three level DTC-IMD with two level DTC-IMD. Significant reduction in steady state torque and flux ripple is observed. Hence, reduced acoustic noise is a distinctive facet of the proposed method.
Keywords: CSVPWM, DTC, MSVPWM, MLI, NPC, VSI

I. INTRODUCTION

In many industrial applications AC drives play a major role. In recent years, studies have been developed to find different solutions for the control of induction motor like V/f control, Field oriented control (FOC), through pulse width modulated voltage source inverter (PWM-VSI). Among these, FOC became popular in the field of high performance drives. Control of induction motor is similar to that of separately excited DC motor using FOC algorithm [1], but in this linear transformation is involved and therefore mathematically intense. To evade this and to achieve decoupled nature, DTC strategy is proposed [2]. Differences flanked by the FOC and DTC has been presented in [3] and finally concluded that DTC gives a good dynamic response. Conventional DTC (CDTC) employs flux and torque hysteresis controllers and so variable inverter switching frequency, ripples in flux and torque particularly in steady state will manifest. To reduce total harmonic distortion (THD) in stator current and to attain constant switching frequency different PWM algorithms have been developed, among which SVPWM gained prominence due to its constant switching frequency operation, maximum DC bus utilisation, ease in digital implementation etc. With the advent of the high frequency power semiconductor devices THD in the inverter output voltage can further reduced with MLI's. Recently MLI's brought renaissance and so NPC three-level inverter [4] is considered in this paper. The pulses generated through MSVPWM algorithm is fed to a three level NPC inverter based DTC-IMD.

With a three phase, two level inverter there are 2^3 switching states and 6 sectors, with three level the possible inverter states are 3^3 and each sector inturn has 6 subsectors, with five level the number of states raise to 5^3 and each subsector inturn will have 6 sub-subsectors with a total of $6*4^2$sub sectors. Reference voltage vector using CSVPWM algorithm is synthesised based on the magnitude (length) and position (sector in which the tip of the reference vector is present). Increasing the number of levels in MLI increases the complexity involved in SVPWM. Hence in this paper a MSVPWM algorithm is proposed in which symmetry of the space vectors is utilized, therby extending the traditional SVPWM approach to a MLI's in [5].

To validate the functionality of the proposed algorithm, three-level inverter fed DTC-IMD is tested under various operating conditions like transient, steadystate, speed reversal and variable load conditions. Also % THD in phase voltage and no-load stator current as a performance measures of the PWM algorithm are analysed, and an improvement of 89.33%, 95.28% are observed.

II. CDTC

The CDTC block diagram is shown in Fig.1. In every sampling time of the inverter stator voltages and currents are sampled. Using these sampled inputs stator flux, speed, torque and flux angle are estimated in the adaptive motor model. Estimated torque and flux are compared with their respective reference values through hysteresis comparators. Based on torque, flux errors and flux angle apt switching state is generated through the optimal switching table. Since none of the inverter switching voltage vector is able to generate the exact stator voltage required to produce the desired changes in torque and flux in most of the switching instances, high ripple in torque, flux and stator current are intrinsic with CDTC. In order to overcome this problem SVPWM based DTC (SVPWM-DTC) is proposed [6]. In this approach the ripples in torque, flux and current are reduced by selecting voltage vectors not for the entire sampling period as in CDTC, but only for a part of the sampling period expressed as switching period and by using zero voltage vector for rest of the period. So, SVPWM-DTC generates a number of voltage vectors higher than that of used in CDTC and so achieves a sensible reduction of ripple in torque, flux and stator current maintaining constant switching frequency.

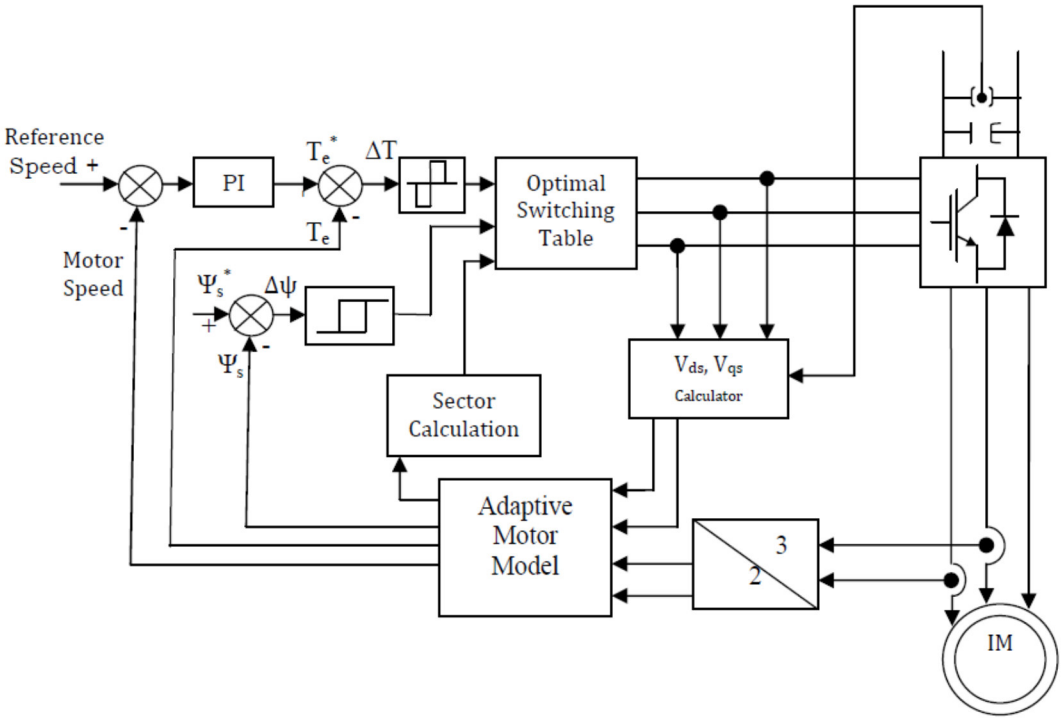


Fig.1 Block diagram of CDTC of induction motor drive

III. CSVPWM STRATEGY FOR TWO LEVEL INVERTER

With a three-phase, two level voltage source inverter (VSI) there are eight possible switching states. Two states, from which no power gets transferred from source to load are termed as null vectors or zero states. The other six states called active states. The active states can be represented by space vectors each of magnitude V_{dc} and divides the space vector plane into six equal sectors as shown in Fig.2. It can be shown that all the six active states can be represented by space vectors given by (1) forming a regular hexagon and dividing the space plane into six sectors each of 60^0, denoted as 1,2,…,6 as shown in Fig.2.

$$V_S = V_{dc} * e^{j(S-1)\Pi/3}, S = 1,2,..,6. \quad (1)$$

In the SVPWM strategy for two level inverter, the desired reference voltage vector is generated by time averaging the two nearby active voltage states and two zero states in every switching period T_S. For a given reference voltage $\overline{V_{ref}}$, the volt-time balance is maintained by applying the active state x, V_x active state y, V_y and two zero states, Zx and Zy together for durations, T_x,T_y and T_Z respectively, as given in (2)

$$T_x = M * \frac{Sin(60^0-\alpha)}{sin60^0} * T_s \quad (2.1)$$

$$T_y = M * \frac{Sin(\alpha)}{sim60^0} * T_s \quad (2.2)$$

$$T_Z=T_s-T_1-T_2 \quad (2.3)$$

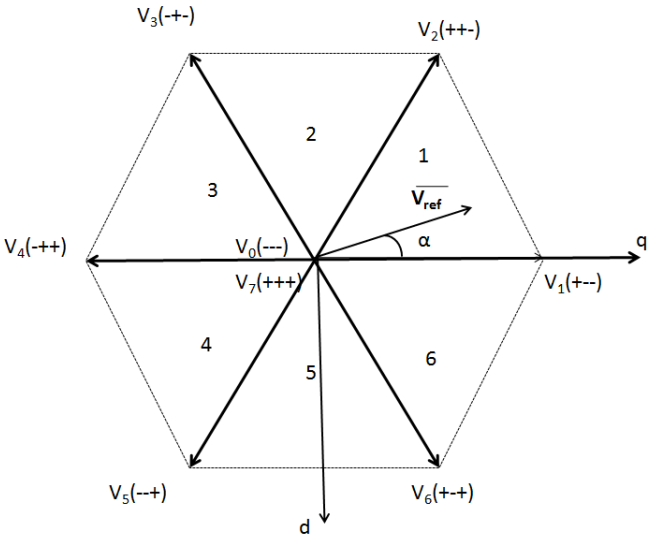


Fig. 2. Switching states and corresponding voltage vectors of a three phase VSI converter. 1,2,3,4,5,6 are the sectors.

Although in CSVPWM strategy the two active vectors and two zero vectors must be applied for durations as in (2), these can be applied in different ways therby creating different sequences[7].

IV. PROPOSED MSVPWM ALGORITHM

A three level NPC inverter is shown in Fig.3. With a three level inverter there are three states corresponding to a zero vector, labeled as V_0, 12 states (pivot states) corresponding to six voltage vectors (pivot vectors) each of magnitude $0.5V_{dc}$ are labeled, V_1-V_6, six states corresponding to six voltage vectors of magnitude $0.866\ V_{dc}$ labeled, V_7-V_{12} and six states corresponding to voltage vectors of magnitude V_{dc} labeled, V_{13}-V_{18} . So with three level VSI there are 27 switching states corresponding to a total of 19 voltage vectors. As explained in the previous section the space plane of two level inverter consists of one zero vector and six active vectors of magnitude V_{dc}. Hence, nearest states are available in case of three level inverter than with that of two level inverter and so reduced voltage ripple with MLI is explicit at all modulation indices. But at the same time two problems manifest with space vector approach to MLI. First one is, identifying the reference vector position interns of subsector/sub-subsector with in a sector and secondly redundancy of voltage vectors of magnitude V_{dc} and $0.5\ V_{dc}$. To offset the associated problems an extended approach to CSVPWM strategy utilize the symmetry of space vectors is considered in this paper.

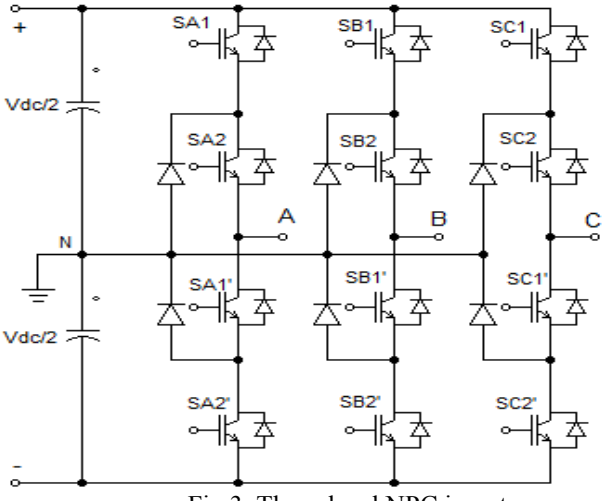


Fig 3. Three-level NPC inverter

The space plane is divided into six sectors, S1-S6 each of 60^0. Each sector is associated with a pivot vector and six other vectors connecting to every subsector. The subsector of S1 are designated as 11,12,13…,16. Similarly subsector of S6 are designated as 61,62,….,66. The switching states and their corresponding voltage vectors, six sectors of a three level inverter are represented in a two dimensional space plane, Fig.4. Switch position, state and pole voltage are shown in Table I. With pivot state as centre the three level space plane can be viewed as six two level hexagons. Each two level hexagon is associated with one pivot vector and six other vectors.

The associated vectors of S1 are represented with solid arrows in Fig.5(a).

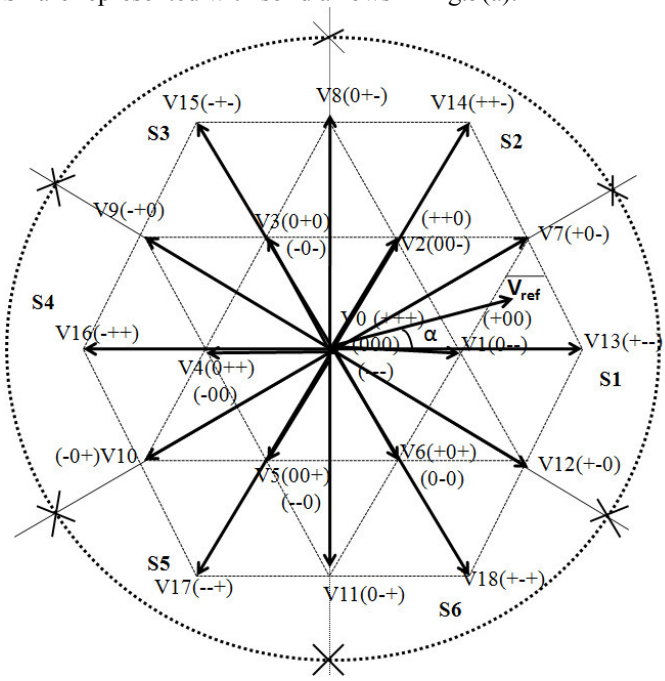


Fig 4. Space vector diagram of 3-level inverter.

Rotating the vectors connected to S1 by 60^0 in the anti-clock wise direction produce space vectors belonging to S2 and shifting the space vectors of S2 by 60^0 produces space vectors of S3 and so on. This is for the reason of symmetry of the six sectors. All the vectors related to any arbitrary sector 'S' can be mapped to S1 using (3). The associated vectors after mapping are shown in Fig.5(b). Let $\overline{V_r}$ is the reference vector to be synthesized. Mapping this vector to S1 reproduces $\overline{V_r}'$ with centre as pivot state corresponding to two level hexagon belonging to S1. The reproduced vector $\overline{V_r}'$ is synthesized by time averaging the mapped nearest three vectors and the dwell times are calculated maintaining the volt-sec balance principle similar to two-level space vector approach. The mapped reference vector and its associated nearest vectors are defined by (3). Identifying the subsector and the dwell times of each state is done as with two-level space vector strategy using (2) replacing V_r,V_x, V_y, V_z, α, T_x, T_y, T_z, V_{dc} with V_r', V_x', V_y', V_z', β, T_x', T_y', T_z', 0.5Vdc. Thus the first problem is resolved using symmetry of the space vectors. Second problem of selecting the apt switching state out of the available redundant states is done based on two criterion. Transition from one state to the next is done with minimum transitions and the last state of a sample must be the first state of the next sample. The switching state selection satisfy's the two criterion is shown in Table II.

$$\overline{V_r'} = \overline{V_{ref}}\, e^{j*(S-1)\Pi/3} - V_1 \quad (3.1)$$

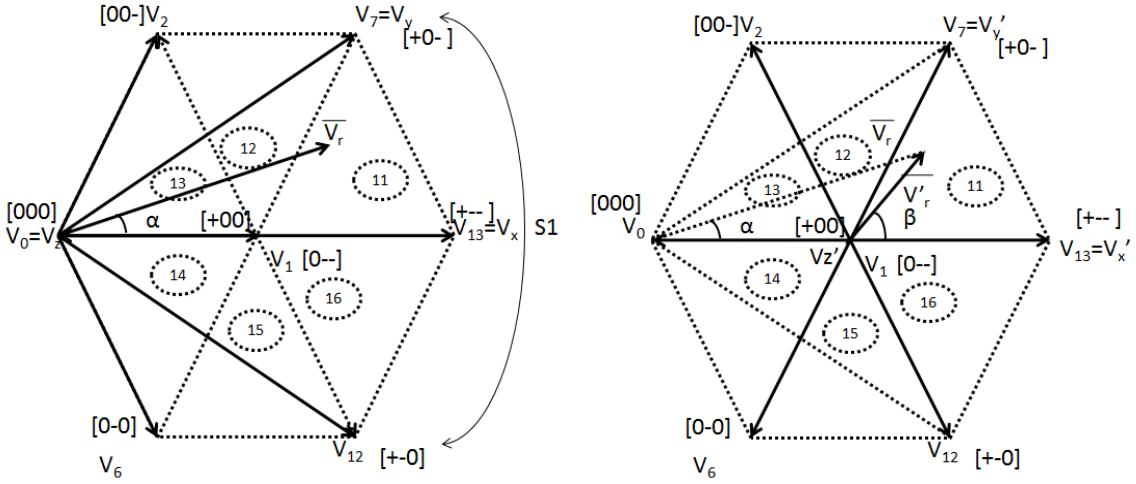
$$\overline{V_x'} = \overline{V_x}\, e^{j*(S-1)\Pi/3} - V_1 \quad (3.2)$$

$$\overline{V_y'} = \overline{V_y}\, e^{j*(S-1)\Pi/3} - V_1 \quad (3.3)$$

$$\overline{V_z'} = \overline{V_z}\, e^{j*(S-1)\Pi/3} - V_1 \quad (3.4)$$

TABLE I
SWITCH POSITION, STATE AND POLE VOLTAGE

Switch Position	**State**	**Pole Voltage ,V_{A0}**
SA1=ON, SA2=ON	+	+Vdc/2
SA1=OFF,SA2=ON	0	0
SA1=OFF,SA2=OFF	-	-Vdc/2



(a) (b)

Fig.5 (a) Reference vector and its associated vectors of S1, (b) Mapped reference vector and its associted vectors of S1

TABLE II STATE SELECTION BASED ON SECTOR AND SUBSECTOR

Sector no.	Subsector No	State-Zx	State-x	State-y	State-Zy
1	1	0--	+--	+0-	+00
	2		00-	+0-	
	3		00-	000	
	4		0-0	000	
	5		0-0	+-0	
	6		+--	+-0	
2	1	++0	++-	0+-	00-
	2		0+0	0+-	
	3		0+0	000	
	4		+00	000	
	5		+00	+0-	
	6		++-	+0-	
3	1	-0-	-+-	-+0	0+0
	2		-00	-+0	
	3		-00	000	
	4		00-	000	
	5		00-	0+-	
	6		-+-	0+-	
4	1	0++	-++	-0+	
	2		00+	-0+	
	3		00+	000	
	4		0+0	000	
	5		0+0	-+0	
	6		-++	-+0	
5	1	--0	--+	0-+	00+
	2		0-0	0-+	
	3		0-0	000	
	4		-00	000	
	5		-00	-0+	
	6		--+	-0+	
6	1	+0+	+-+	+-0	0-0
	2		+00	+-0	
	3		+00	000	
	4		00+	000	
	5		00+	0-+	
	6		+-+	0-+	

VI. PROPOSED MSVPWM ALGORITHM BASED 3-LEVEL INVERTER FED DTC-IM DRIVE

The block diagram of the proposed DTC-IMD is shown in Fig.6. The reference voltage space vector can be synthesized in many ways. In SVPWM based DTC method, instead of torque and flux hysteresis controllers, proportional + integral (PI) controllers and reference voltage vector calculator are used to determine the reference voltage vector. The required reference voltage vector, to control the torque and flux cycle-by-cycle basis is constructed by using the errors between the reference d-axis and q-axis stator fluxes and d-axis and q-axis estimated stator fluxes sampled from the previous cycle.

The position of the reference stator flux vector $\overline{\Psi_s}^*$ is derived by adding the slip speed derived from the torque controller and the actual rotor speed estimated by the adaptive motor model. After each sampling interval, actual stator flux vector $\overline{\Psi_s}$ is corrected by the error and it tries to attain the reference flux space vector $\overline{\Psi_s}^*$. Reference values of the d-axis and q- axis stator fluxes and actual values of the d-axis and q-axis stator fluxes are compared in the reference voltage vector calculator (RVVC) block and hence the errors in the d-axis and q-axis stator flux vectors are obtained using (4).

$$\Delta\Psi_{ds} = \Psi_{ds}^* - \Psi_{ds} \quad (4.1)$$

$$\Delta\Psi_{qs} = \Psi_{qs}^* - \Psi_{qs} \quad (4.2)$$

The knowledge of flux error and stator ohmic drop allows the determination of appropriate reference voltage space vectors using (5). where, Further, these d-q components of the reference voltage vector are fed to the MSVPWM block in which, the actual switching times for each inverter leg are calculated and the respective pulses are generated to synthesize the reference voltage vector in an average sense with in a subcycle.

$$V_{ds}^* = R_s i_{ds} + \frac{\Delta\Psi_{ds}}{T_s} \quad (5.1)$$

$$V_{qs}^* = R_s i_{qs} + \frac{\Delta\Psi_{qs}}{T_s} \quad (5.2)$$

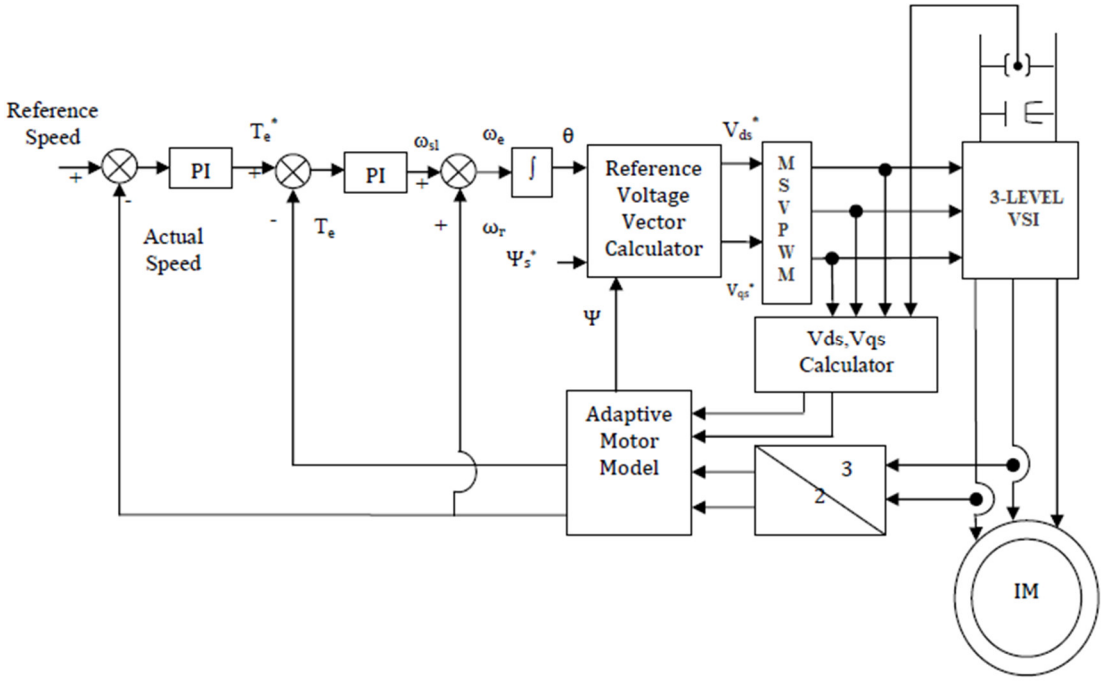


Fig.6 Block diagram of the proposed DTC IM drive

VII. SIMULATION RESULTS AND DISCUSSIONS

The performance of the MSVPWM based DTC-IMD is tested in Matlab/Simulink environment. The mathematical simulation has been carried out with fixed step size of 1μs using ode4 (Runge-Kutta) solver. The parameters of the motor considered for simulation is given in Table III. The steady state response of CDTC-IMD, phase voltage and stator current with harmonic spectra are shown in Fig.7 to Fig.9. The 2-level inverter fed DTC-IMD the steady state response, phase voltage and stator current harmonic spectra are analysed with reference to Fig.10 to Fig.12. The performance of 3-level inverter based DTC-IMD is analysed during the steady state, transient, speed reversal and step change in load Fig.13. to Fig.18. The quantitative analysis of % reduction in THD with CDTC as reference, is tabulated in Table IV.

TABLE III PARAMETERS OF THE MOTOR

PARAMETER	RATING
Stator resistance, Rs	7.83Ω
Rotor resistance, Rr	7.55Ω
Stator Inductance, Ls	0.4751H
Rotor Inductance, Lr	0.4751H
Mutual Inductance, Lm	0.4535H
Moment of inertia, J	0.06 Kg.m^2
Number of poles, P	4

TABLE IV % REDUCTION IN THD

METHOD	%VTHD	% Reduction in VTHD	%ITHD	% Reduction in ITHD
CDTC-IMD	180.9	0	23.54	0
2-level DTC-IMD	34.17	81.11	2.15	90.86
3-level DTC-IMD	19.29	89.33	1.11	95.28

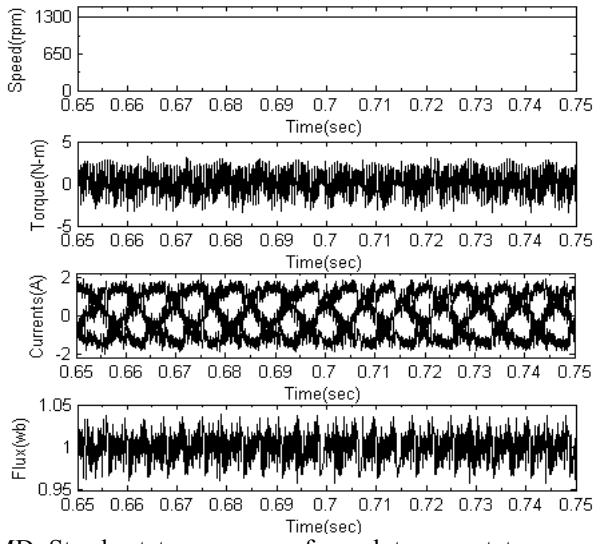


Fig.7 CDTC-IMD: Steady state response of speed, torque, stator currents and stator flux

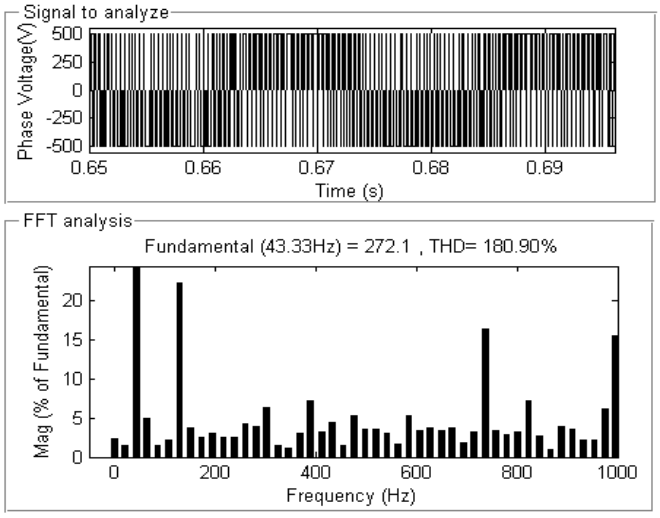


Fig.8 CDTC-IMD: Phase voltage with its harmonic spectrum

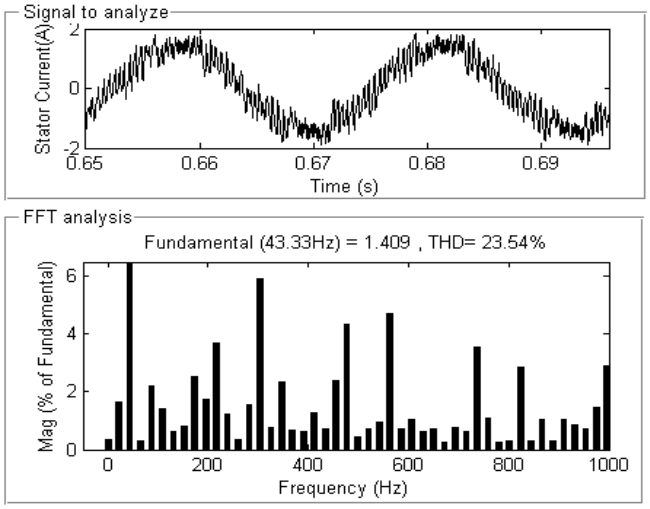


Fig.9 CDTC-IMD: Stator current with its harmonic spectrum

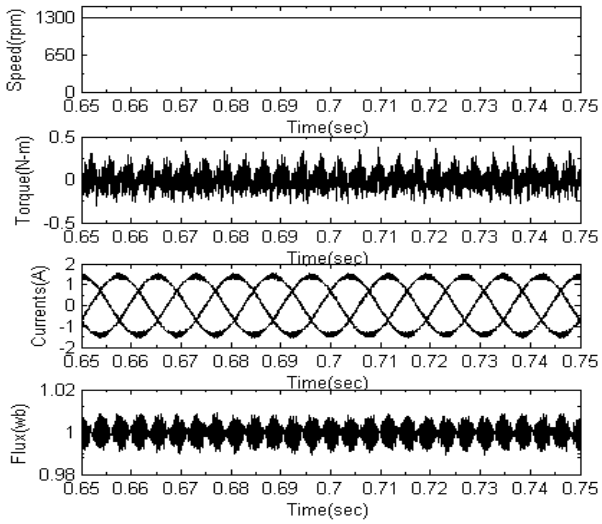


Fig.10 Two-level SVPWM based DTC-IMD: Steady state response of speed, torque, stator currents and stator flux

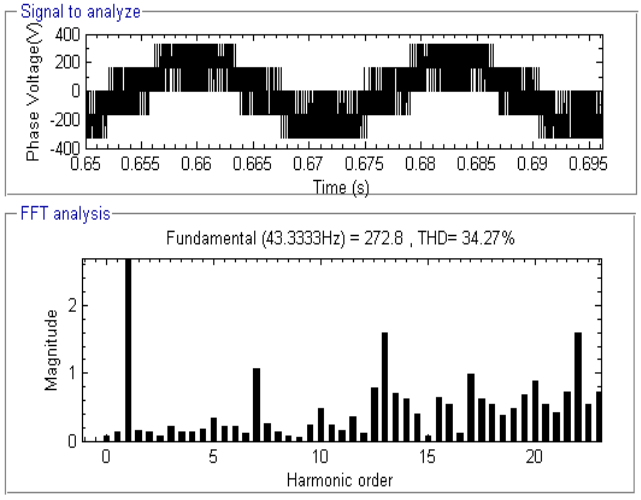


Fig.11 Two-level SVPWM based DTC-IMD: Phase voltage with its harmonic spectrum

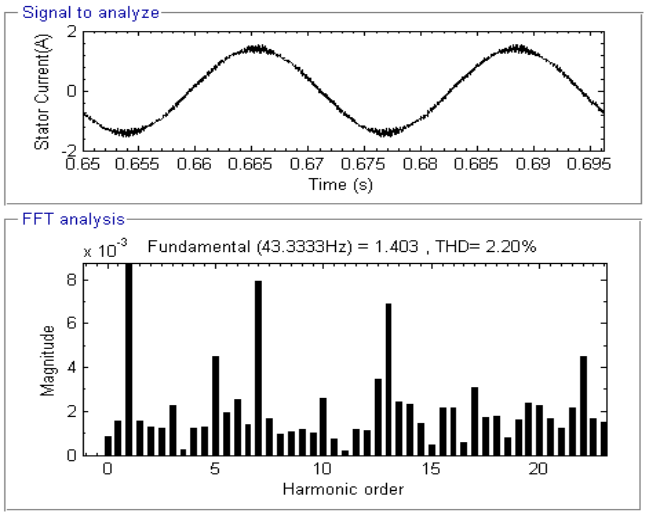


Fig.12 Two-level SVPWM based DTC-IMD: Stator current with its harmonic spectrum

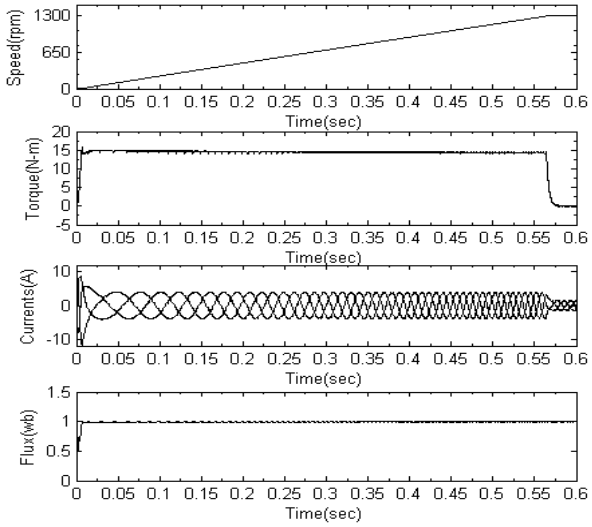


Fig.13 Three-level MSVPWM based DTC-IMD: Starting transient response of speed, torque, stator currents and stator flux

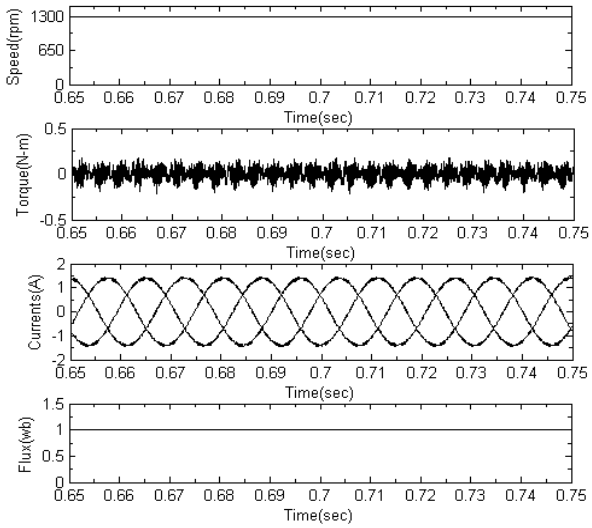


Fig.14 Three-level MSVPWM based DTC-IMD: Steady state response of speed, torque, stator currents and stator flux

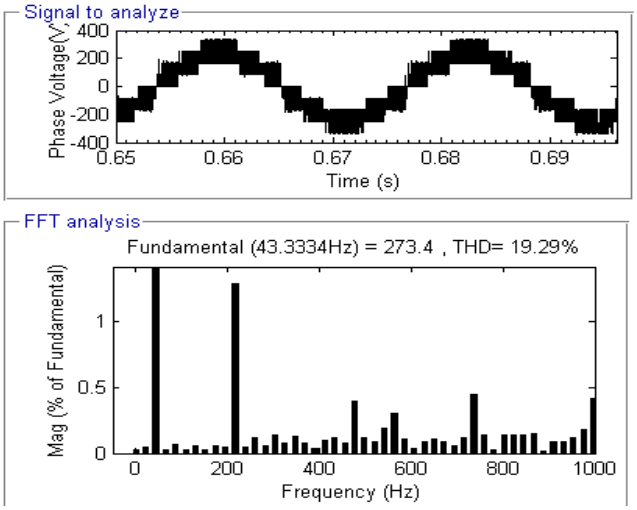


Fig.15 Three-level MSVPWM based DTC-IMD: Phase voltage with its harmonic spectrum

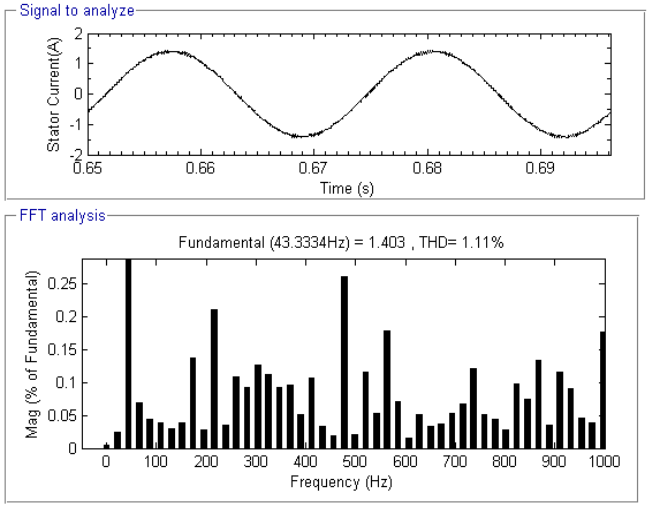


Fig.16 Three-level MSVPWM based DTC-IMD: Stator current with its harmonic spectrum

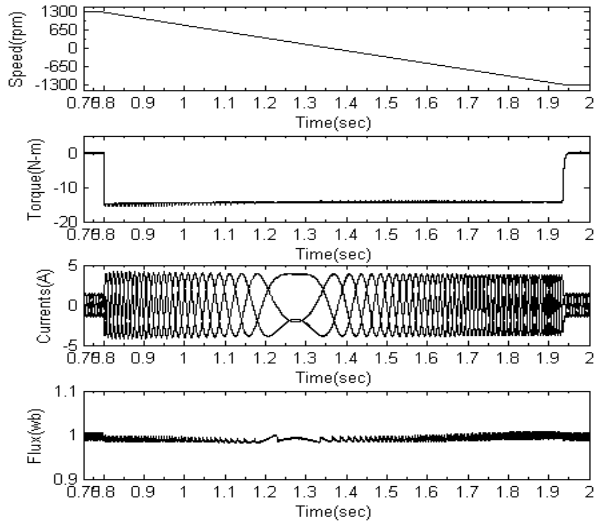


Fig.17 Three-level MSVPWM based DTC-IMD: Transients in speed, torque, stator currents and stator flux during speed reversal (speed is changed from 1300rpm to -1300rpm)

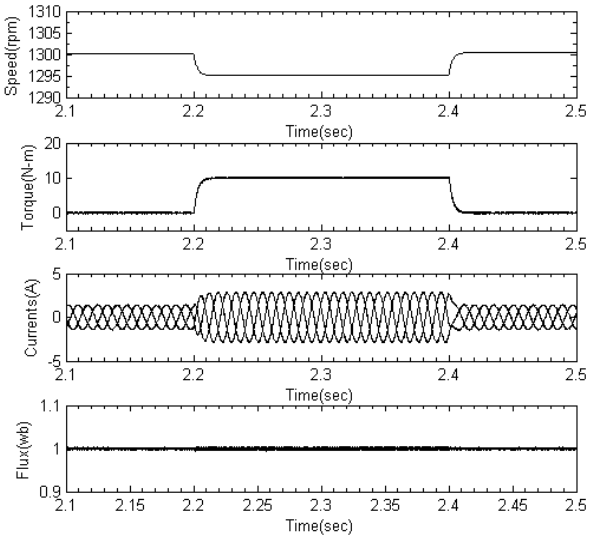


Fig.18 Three-level MSVPWM based DTC-IMD: Transients in speed, torque, stator currents and stator flux during step change in load (10N-m is applied from 2.2sec to2.4sec)

VII. CONCLUSIONS

In this paper, a Modified SVPWM algorithm for three-phase three-level inverter fed DTC-IMD is proposed. MSVPWM algorithm generates switching pulses for three-level inverter similar to that of a two-level inverter utilising the symmetry of the voltage vectors. Thus, MSVPWM algorithm reduces the complexity involved in MLI driven with SVPWM algorithm. To validate the performance of three-level MSVPWM inverter fed DTC-IMD, mathematical simulation has been carried out and the results are presented. From the simulation results, it is concluded, that the MSVPWM algorithm for three-level inverter fed DTC IMD gives good dynamic response, reduced steady state ripples and total harmonic distortion.

REFERENCES

[1] F. Blaschke "The principle of field orientation as applied to the newtransvector closed loop control system for rotating field machines," *Siemens Review*, 1972, pp 217-220.

[2] Isao Takahashi and Toshihiko Noguchi, "A new quick-response andhigh-efficiency control strategy of an induction motor," *IEEE Trans.Ind. Applicat.*, vol. IA-22, no.5, Sep/Oct 1986, pp. 820-827.

[3] Domenico Casadei, Francesco Profumo, Giovanni Serra, and AngeloTani, "FOC and DTC: Two Viable Schemes for Induction MotorsTorque Control" *IEEE Trans. Power Electron.,* vol. 17, no.5, Sep, 2002,pp. 779-787.

[4] Nabae, A., Takahashi, I., and Akagi, H, "A neutral-point clamped PWMinverter', *IEEE-Trans. Ind. Appl.*, 1981, 17, (5), pp.518-523.

[5] Abdul Rahiman Beig, G. Narayana, V.T. Ranganathan, "Modified SVPWM Algorithm for Three Level VSI With Synchronized and Symmetrical Waveforms", *IEEE Trans. Ind. Elect.*, Vol. 54, No. 1, Feb.2007, pp 486-494.

[6] C.Hari Krishna, J.amarnath and S.Kamakshaiah "Simplified SVPWM Algorithm for Neutral Point Clamped 3-level Inverter fed DTC-IM Drive*" In proc IEEE Adv. Pow. (APCET) ,conf* 2012.pp 1-6

[7] S.Das and G.Narayanan, "Novel switching sequences for a space-vector modulated three-level inverter", *IEEE Trans.Ind. Electron*.,vol.59, no.3,pp.1477-1487, March 2012.

BIOGRAPHIES

B.Pradeep Kumar Reddy is born in 1989 in India. He has graduated from Vivekananda Institute of Technology and Sciences, Karimnagar in 2010. Presently he is pursuing post graduation in Power electronics Specialization at RGM College of engineering and Technology, Nandyal. His areas of interest include Power electronics, Drives and Control and Pulse Width Modulation Techniques.

G. Kumaraswamy is born in 1983 in India. He is graduated from JNT University in 2005 and pursued Post graduation from the same university. He is currently working as an Associate professor in the department of electrical and electronics engineering, R.G.M College of engineering and technology, Nandyal, Andhra Pradesh, India. He has nine years of teaching experience. He has attended several National workshops. His main areas of research include Power Electronics, Pulse Width Modulation Techniques, Drives and Control and multilevel inverters.

Dr. K.Sri Gowri received the B.Tech degree from SVU college of Engineering, Tirupati in1997, the M.Tech degree from RGM College of Engineering and Technology, Nandyal and has been awarded Ph.D in the area of Power Electronic Control of Electric Drives from JNTU Kakinada in 2010. She is currently working as Professor and HOD in the Department of EEE at RGMCET, Nandyal, A.P. Her areas of interest include Power Electronics, Pulse Width Modulation Techniques, Drives and Control and Renewable Sources of Energy.