Novel Low Power and Low Transistor Count Flip-Flop Design with High Performance

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Abstract

The paper proposed a new design of static SET flip-flop for low power applications. In this work, comparative analysis of existing architecture for flip-flops along with the proposed design is made. The comparison is done on the basis of power and power delay product, transistor count is also included. Due to continuous increase in integration of transistors and growing needs of portable equipments, low power design is of prime importance. The proposed design has the best power and the second best PDP than the existing architectures. Proposed FF has the least transistor count hence reducing the manufacturing cost and area. All simulations are performed on TSpice using BSIM models in 130 nm process node. The simulation results show that for all supply voltages, proposed FF has the best power consumption, second best PDP and the lowest transistor count. So this design is best suited for low power and high performance portable applications.

Keywords: Transmission Gate, Short circuit current, Edge Triggered*,* Optimization

1. INTRODUCTION

The latest advances in mobile battery-powered devices such as the Personal Digital Assistant (PDA) and mobile phones have set new goals in digital VLSI design. The portable devices require high speed and low power consumption. So the power dissipation has become a prominent issue [1]. Flip-flops are widely used in digital circuits to store data. Of the various building blocks in digital designs, flip flop is the most complex and power consumer [2]. Flip-flops are often used in computational circuits to operate in selected sequences during recurring clock intervals to receive and maintain data for a limited time period sufficient for other circuits within a system to further process data. The power, delay, and reliability of the flip-flops directly affect the performance and fault tolerance of the whole electronic system [3]. Therefore, it is imperative to carefully design flip flops for minimum area, delay, power, and maximum reliability. Several flip-flop designs have been proposed for power reduction. Some of these designs require a large number of transistors for implementation, resulting in a large area, not necessarily suitable for small, low-priced systems. In this work, we extensively studied the existing flip-flop architectures, compared them, analyzed their weaknesses and proposed new high performance, low power and low transistor count single edge triggered flip-flop.

In Section II of this paper, previously published state-of-the-art single-edge triggered flip-flops (SETFFs) are reviewed. Section III presents the structure and operating principle of the proposed design. In Section IV, the nominal simulation conditions, along with analysis and optimization performed during simulation, are discussed. In Section V, results are presented and performance for new proposed design and conventional designs are compared in terms of power, PDP and transistor count.   Finally, paper ends with conclusion in Section

VI. EXISTING SINGLE EDGE TRIGGERED FLIP-FLOPS

2.1 Push Pull Flip-Flop

Push Pull Flip-flop (PPFF) is shown in Fig. 2. To improve the performance of a conventional TGFF (shown in Fig. 1), addition of an inverter and transmission gate was proposed by [4] between the outputs of master and slave latches to accomplish a push–pull effect at the slave latch. This increased 4 transistors. To compensate this increment of transistor count, Push Pull Flip-Flop eliminated two transmission gates from the feedback paths of conventional TG FF.

2.2 Ten Transistor Flip-Flop

The 10-transistor single edge triggered flip-flop proposed by [5], is illustrated in Fig. 3. This flip-flop has lesser transistor count as compare to other discussed flip-flops in this section. In this design the feedback circuit of the master section is removed and in slave section, feedback loop consists of transmission gate. When clock level is 'HIGH', master latch is functional and the inverse of the data is stored to an intermediate node N. When the clock goes to 'LOW' logic level, the slave latch becomes functional and produces data at the output Q and QB.

2.3 Low Area Flip-Flop

To reduce the area of the conventional TGFF, [6] removed the two feedback transmission gates of conventional TG FF. This low-area DFF is shown in Fig. 4. When clock level is 'HIGH', master latch is functional and the inverse of the data is stored to an intermediate node N. When the clock goes to 'LOW' logic level, the slave latch becomes functional and produces data at the output Q.

2. PROPOSED SINGLE EDGE TRIGGERED FLIP-FLOP

The new SET flip-flop structure is proposed in this paper. The proposed flip-flop (Proposed FF) is shown in Fig. 5. This flip-flop is the modification over Low Area Flip-Flop proposed by [6]. The feedback path is improved in our flip-flop. Low Area Flip-Flop proposed by [6] used two feedback loops one each in the master as well as the slave stage, which increased the total parasitic capacitance at the internal flip-flop nodes, leading to higher dynamic power dissipation and reduced performance. In proposed flip-flop, the inverter of feedback circuit of the master section is removed. This improved the power efficiency and speed of our flip-flop and the flip-flop remain static in nature. The proposed Flip-Flop has better power performance, lesser delay, PDP and area as compare to Low Area Flip-Flop. So the novelty of the proposed Flip-Flop lies in the feedback strategy used to make the design static using lesser number of transistors. In proposed Flip-Flop when clock level is 'HIGH', master latch is activated and inverse of the data is stored to an intermediate node N. When clock goes to 'LOW' logic level, the slave latch becomes functional and produces data at the output Q.

3. SIMULATION

Simulation parameters used for comparison, are shown in table I.

Under nominal condition, a 16-cycle sequence (1111010110010000) with an activity factor of 18.75% is supplied at the input for average power measurements. Power consumption based on pseudorandom data sequence of 18.75% was considered as the real parameter for characterizing power dissipation of a flip-flop design.

The dynamic power consumption is dependent on switching activities at various nodes of the circuit. It varies with different data rates and circuit topologies. Hence to obtain a fair idea of power dissipation for a circuit topology, different data patterns should be applied with different activity rates [7]. So in the following simulations, following four different data sequences have been adopted to compare the power consumption of flip-flop structures discussed in this paper:

i)   1111111111111111 (A=0)

ii)   1111010110010000 (A=0.18)

iii)   1100110011001100 (A=0.5)

iv)   1010101010101010 (A=1)

Where "A" is the data activity. The results are carried out for the period of 16 data sequences. All simulations are performed on TSpice using BSIM 3v3 level 53 models in 130 nm process node. The supply voltage is varied from 1.6V to 2V. The clock frequency is varied from 100MHz to 1GHz.

4.1 Analysis

The flip-flops can be compared at various parameters. In general, a PDP-based comparison is appropriate for low power portable systems. In this paper, our main interest is in SETFF usage for low-power applications. Therefore power consumption is selected for comparing different flip-flops. Additionally we also compared PDP and transistor count of the discussed flip-flops.

3.2 Optimization

There is always a tradeoff between power dissipation and propagation delay of a circuit. A flip-flop can be optimized for either high performance or low power but both the parameters are critical, the designs are simulated to achieve minimum power in this work. PDP and transistor count are also included to maintain a fair level of comparisons.

The feedback path is improved in the proposed flip-flop. Most of the conventional static designs used two feedback loops one each in the master as well as the slave stage, which increased the total parasitic capacitance at the internal flip-flop nodes, leading to higher dynamic power dissipation and reduced performance. This also resulted in total chip area overhead due to increased transistor count [8]. In proposed flip-flop, the inverter of feedback circuit of the master section is removed. This improved the power efficiency and speed of our flip-flop and the flip-flop remain static in nature. The proposed Flip-Flop has better power performance, lesser delay, PDP and area as compare to Low Area Flip-Flop. The transistors, that are not located on critical path, are implemented with minimum size to reduce area overhead and to minimize power dissipation. In proposed design, device count is reduced and parasitic capacitances at internal nodes of the flip-flops are decreased that results in improved power dissipation. We have also reduced the number of clocked transistors. Thus the power is further reduced.

4.   RESULT AND DISCUSSION

Figure 6 shows the power consumption as a function of supply voltage. This shows that power increases with the increase in supply voltage. The simulation results indicate that the proposed Flip-Flop has the least power dissipation for all supply voltages. Table II indicates the power consumption in microwatts at different supply voltages for 18.75% data activity and 400MHz clock frequency. For fair comparison, the average of power consumption at all voltages is taken. The proposed Flip-Flop has 59.47%, 8.63% and 8.27% lesser average power dissipation when compared to the 10 Transistor Flip-Flop proposed by [5], PPFF and Low Area FF respectively. Among previously published flip-flops at 1.6V, PPFF has the best power dissipation but as the voltage increases the power dissipation of PPFF increases. At 1.8V and 2.0V, Low Area FF shows better power dissipation than PPFF and 10 Transistor Flip-Flop proposed by [5]. Overall among previously proposed Flip-Flops, Low Area FF has the best power dissipation and Flip-Flop proposed by [5] has the worst power dissipation.

Table III shows power consumption in microwatts as a function of clock frequency.   Figure 7 show that, all flip-flops consume larger power at 1GHz clock frequency and lesser power for 100MHz clock frequency. So, as clock frequency increases, power consumption increases. For 100 MHz, 250 MHz and 400 MHz clock frequencies proposed flip-flop shows the lowest power consumption. For 200 MHz and 1GHz clock frequencies, PPFF shows the best power consumption. For all clock frequencies, flip-flop proposed by [5] shows the highest power consumption. For fair comparison, the average of power consumption at all clock frequencies is taken. This average result shows

that the proposed flip-flop has 39.71% and 18.17% improvement in average power consumption when compared to the existing 10 Transistor flip-flop proposed by [5] and Low Area FF respectively. However proposed Flip-Flop consumes 0.32% more power than PPFF, which is very small percentage. So Proposed FF and PPFF consume almost same power. Overall 10 Transistor flip-flop proposed by [5] consumes the highest power and Proposed FF and PPFF consume the lowest power.

Fig. 8 shows, 100% data activity exhibits the largest power consumption and 0% data activity exhibits the smallest power consumption. The proposed FF shows the best power performance for all switching activity except zero switching activity. For this zero switching activity, Low Area FF shows the best power performance and proposed FF shows the second best power performance. Power consumption in µW as a function of data activity is shown in Table IV. For fair comparison, we took the average of power consumption at all data activities. This average result shows that the proposed FF has 40.46%, 14.02% and 3.09% improvement in average power consumption when compared to the previously published 10 Transistor flip-flop proposed by [5], Low Area FF and PPFF respectively. Ten transistor flip-flop proposed by [5] consumes the highest power for all switching activity. For 0 switching activity, Low Area FF is better while for all other cases PPFF is better than all other previously proposed flip-flops.

Table V shows clock to Q PDP for different flip-flops as a function of supply voltage. For all voltages PPFF shows the best PDP except 1.6V. At 1.6V proposed FF has the best PDP. Over all PPFF shows the best PDP. The proposed FF shows the second best PDP. For fair comparison, the average of PDP at all voltages is taken. This average result shows that the proposed FF has 35.87% and 12.38% better PDP when compared to the previously proposed Low Area FF and 10 Transistor flip-flop proposed by [5], respectively. However proposed FF has 4.51%larger PDP than PPFF. Low Area FF has the worst PDP.

Table VI illustrates the transistor count for the various flip-flop designs discussed in this paper (excluding the inverter to generate the complementary clock signals). Proposed FF design is composed of only ten transistors and has the least transistor count and the lowest clocked transistor among all the previously proposed static flip-flops. It is further seen that PPFF has the largest transistor count. PPFF requires 6 more transistors and 2 more clocked transistors than the proposed design. Low Area FF requires 2 more transistors than the proposed design. 10 transistor flip-flop proposed by [5] also has same transistor count as proposed FF but proposed FF has up to 59.47%, better average power dissipation and 12.38% better PDP than the 10 transistor flip-flop proposed by [5].

5. CONCLUSION

A comparative analysis of single edge triggered flip-flops has been done. The new flip-flop structure has been proposed in this paper. The proposed flip-flop structure is compared on the basis of power, PDP and transistor count with the existing flip-flop structures. For all supply voltages the proposed FF has the best power consumption and has up to 59.47% improvement in power. The average of power consumption at all clock frequencies shows that the proposed FF has almost the best power consumption and has up to 39.71% improvement in power. The proposed FF shows the best power performance for all switching activity except zero switching activity, for this zero switching activity, Low Area FF shows the best power performance and proposed FF shows the second best power performance. The average result of power consumption at all data activities shows that the proposed FF has up to 40.46% improvement in average power consumption. The proposed FF shows the second best PDP and has up to 35.87% improvement in PDP. Proposed FF design is composed of only ten transistors and has the least transistor count and lowest clocked transistor among all the previously proposed static flip-flops.

Among previously published flip-flops, PPFF has the largest transistor count but overall PPFF has the best power dissipation and the best PDP. For all voltages and all clock frequencies, FF proposed by [5] shows the highest power consumption. 10 transistor flip-flop proposed by [5] also has same transistor count as proposed FF but proposed FF has up to 59.47%, better average power dissipation and 12.38% better PDP than the 10 transistor flip-flop proposed by [5]. Among all flip-flops compared, the proposed FF is found to be the best energy efficient having the second best PDP with the lowest transistor count. The proposed FF has up to 59.47% improvement in power and up to 35.87% improvement in PDP. So, proposed FF is best suited for low power and high performance

applications where area is also of prime concern.

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S. No.	1	2	3	4	5	6	7	8	9	10	11
Particulars	CMOS Technology	Min. Gate Width	Max. Gate Width	MOSFET Model	Nominal Supply Voltage	Temperature	Duty Cycle	Nominal Clock Frequency	Sequence Length	Rise Time of Clock & Data	Fall Time of Clock & Data
Value	130 nm	260 nm	1.04 μm	BSIM 3v3 level 53	1.6V	25° C	50 %	400MHz	16 Data Cycles	100 ps	100 ps

Table I: CMOS Simulation Parameters

VDD (V)	PPFF	Low Area FF	10 Transistor FF Proposed by [5]	Proposed FF
1.6	10.1	11.8	16.2	9.47
1.8	12.4	11.9	26.6	11.69
2.0	15.4	14.05	42.6	13.45
Average	12.63	12.58	28.47	11.54

Table II: power consumption in μW as a function of supply voltage

CLOCK (MHz)	PPFF	Low Area FF	10 Transistor FF Proposed by [5]	Proposed FF
100	6.16	8.77	12.2	6.04
200	7.09	9.74	13.52	7.44
250	8.36	9.21	14.23	7.62
400	10.1	11.8	16.22	9.47
10000	15.42	18.28	22.27	16.74
Average	9.43	11.56	15.69	9.46

Table III: Power consumption in μW as a function of clock frequency

Data Activity	PPFF	Low Area FF	10 Transistor FF Proposed by [5]	Proposed FF
0%	5.14	4.49	15.8	4.52
18.75%	10.1	11.8	16.22	9.47
50%	9.89	11.61	16.05	9.77
100%	15.22	18.72	20.78	14.57
Average	9.05	10.20	14.73	8.77

Table IV: Power Consumption in µW as a function of data activity

Vdd (v)	PPFF 10^{-18}J	Low Area FF 10^{-18}J	10 Transistor FF Proposed by [5] 10^{-18}J	Proposed FF 10^{-18}J
1.6	1337.24	3367.25	1591.65	1317.61
1.8	1385.7	1871.99	1553.44	1603.4
2.0	1467.62	1604.3	1863.75	1467.80
Average	1396.9	2281.2	1669.61	1462.9

Table V: PDP_{C_Q} as a function of supply voltage

Flip-Flop	PPFF	Low Area FF	10 Transistor FF Proposed by [5]	Proposed FF
No of transistors	16	12	10	10
No of clocked transistors	6	4	4	4

Table VI: Transistor count of various flip-flops
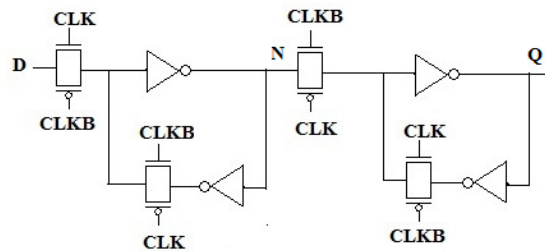
Fig 1: Conventional TG FF
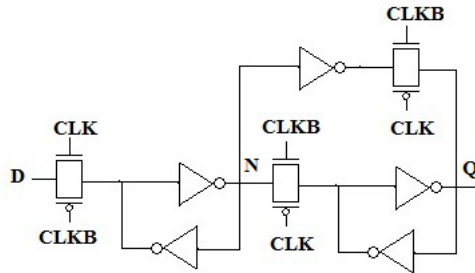
Fig 2: Push Pull Flip-Flop (PPFF)
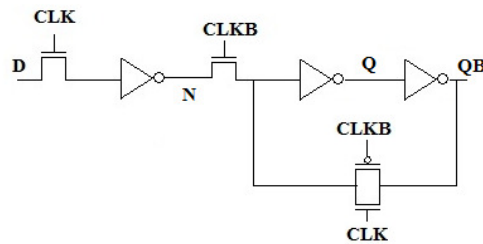
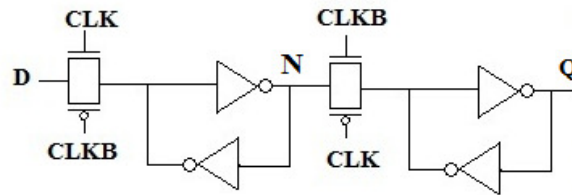Fig 3: 10 Transistors Flip-Flop Proposed by [5]
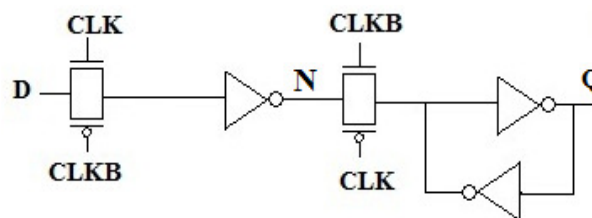
Fig 4: Low Area Flip-Flop

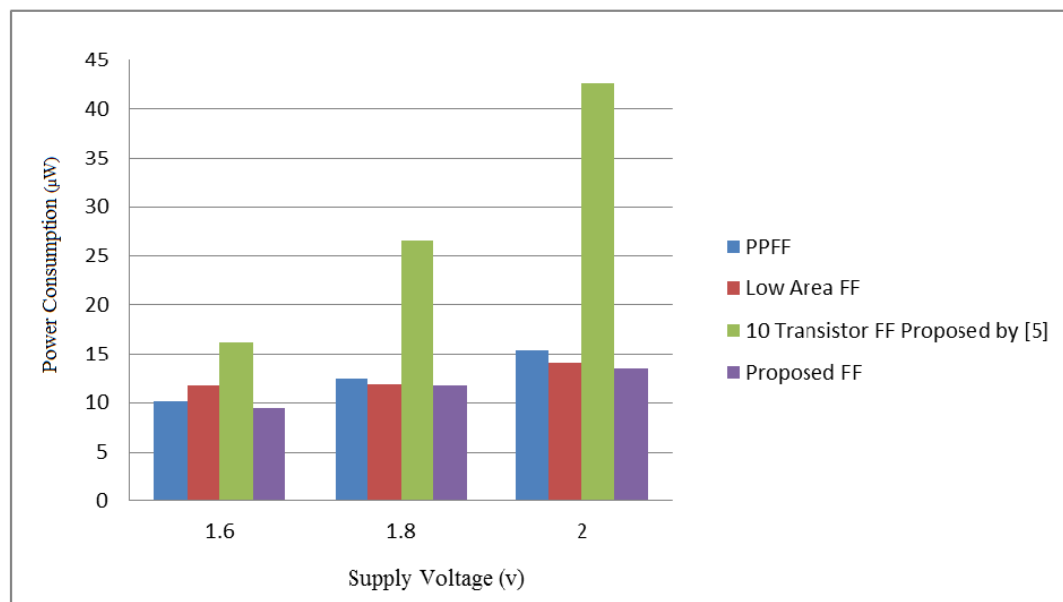
Fig 5: Proposed Flip-Flop

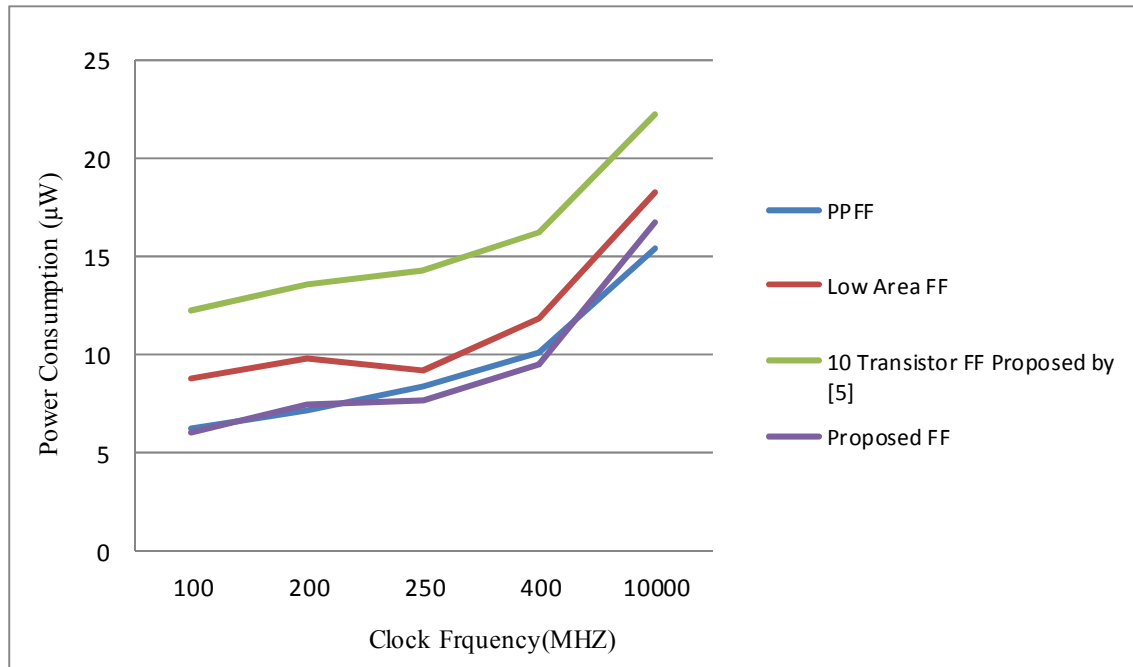Fig 6: Power consumption as a function of supply voltage

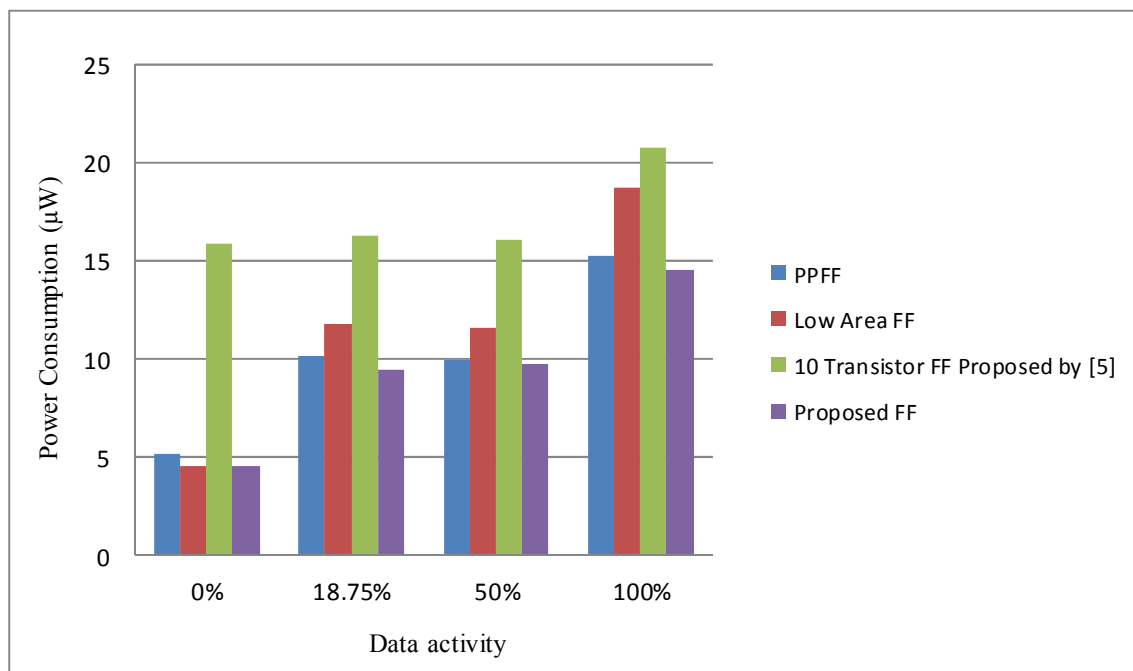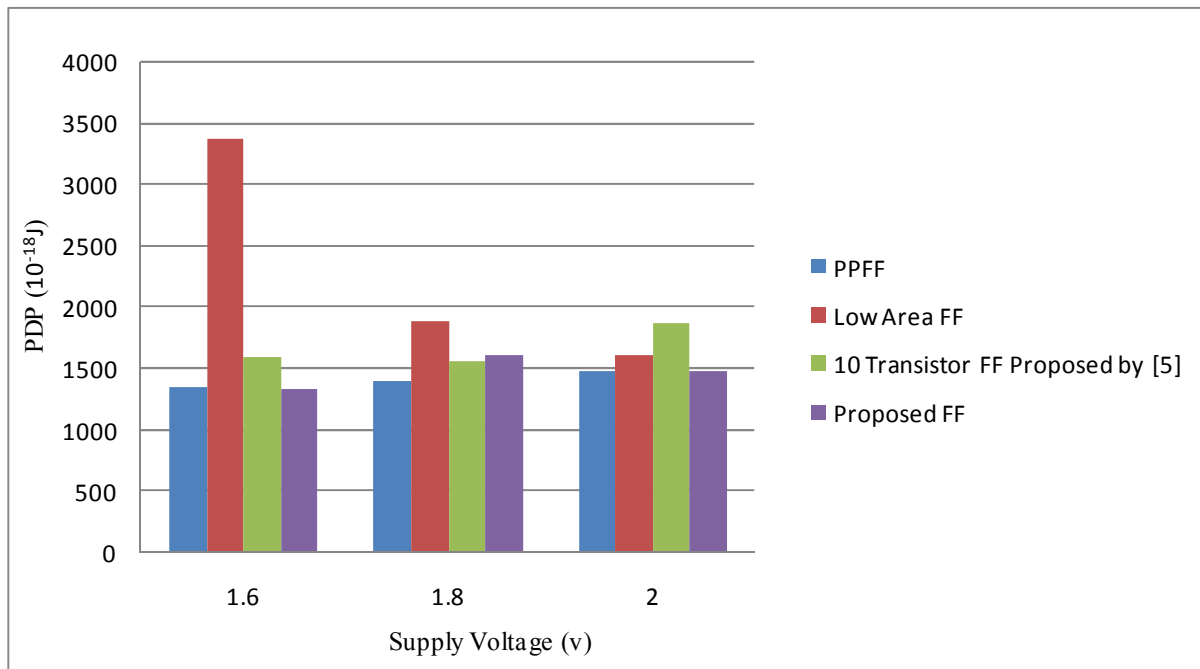Fig. 7:   Power Consumption as a function of clock frequency

Fig 8: Power consumption dependence on data activity rates

Fig 9: PDP dependence on supply Volta