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Proposed Thermal Circuit Model for the Cost Effective Design of Fin FET

A K M Kamrul Hasan, MD. Nizamul Islam, Dewan Siam Shafiullah
Islamic University of Technology (IUT)
Gazipur, Bangladesh.

Abstract

The Complementary metal-oxide-semiconductor (CMOS) device has been rapidly evolving and its size has been drastically decreasing ever since it was first fabricated in 1960 [Us Patent 3,356,858: 1967]. The substantial reduction in the CMOS device size has led to short channel effects which have resulted in the introduction of Fin Field Effect Transistor (FinFET), a tri-gate transistor built on a silicon on insulator (SOI) substrate. Furthermore, due to the geometry of the FinFET the severity of the heating problem has dramatically increased. Self-heating in the 3-dimensional FinFET device enhances the temperature gradients and peak temperature, which decrease drive current, increase the interconnect delays and degrade the device and interconnect reliability. In this work we have proposed a methodology to develop an accurate thermal model for the FinFET through a rigorous physics-based mathematical approach. A thermal circuit for the FinFET will be derived from the model. This model will allow chip designers to predict interconnect temperature which will lead them to achieve cost-effective design for the FinFET-based semiconductor chips.

Keywords: Bulk CMOS, SOI CMOS, FinFET, Thermal heating.

1. Introduction

Majority of integrated circuits produced in CMOS technology are based on a pair of complementary MOSFETs including n-channel and p-channel field effect transistors. The n-channel device employs a sufficiently high positive voltage to the gate with respect to the source, and electrons are then attracted to the semiconductor surface to establish a conductive n-channel between the source and drain, making current flow possible. The gate voltage necessary to form the channel is called the threshold voltage (V_T). However, the p-channel device requires a negative gate voltage for a conductive p-channel. Over the past 15 years, the number of devices in a single chip is approximately doubled, and the number density of devices has been significantly increased. Thus, the power density has been increasing rapidly, approaching air cool limit. The transistor channel length has decreased almost 3 orders of magnitude in approximately 30 years. However, the reduction of horizontal dimensions (such as gate length and metal width) must be accompanied by an appropriate reduction of vertical ones (such as oxide gate thickness and device channel thickness), as well as increased doping and lowered supply voltage [1]. The negative effects of failing to meet these criteria will be explained in greater detail later in this proposal.

2. Advantages of SOI CMOS over Bulk CMOS

The term SOI means Silicon On Insulator structure, which consists of devices on silicon thin film (SOI layers) that exists on insulating film. Figure1 illustrates an outline sketch of bulk, partial depletion type and complete depletion type SOI-MOS (Metal Oxide Semiconductor) transistor structure. In the case of bulk CMOS devices, P/N type MOS transistors are isolated from the well layer. In contrast, SOI-CMOS devices are separated into Si supporting substrate and buried oxide film (BOX). Also, these devices are structured so each element is completely isolated by LOCOS (Local Oxidation of Silicon) oxide film and the operating elements area (called the SOI layer) is completely isolated by insulators. Also, elements that have a thin SOI layer (normally <50 nm) and have all body areas under the channel depleted, are called complete depletion type SOI. Conversely, elements that have a thick SOI layer (normally >100 nm) and have some areas at the bottom of the body area that are not depleted, are called partial depletion type SOI.

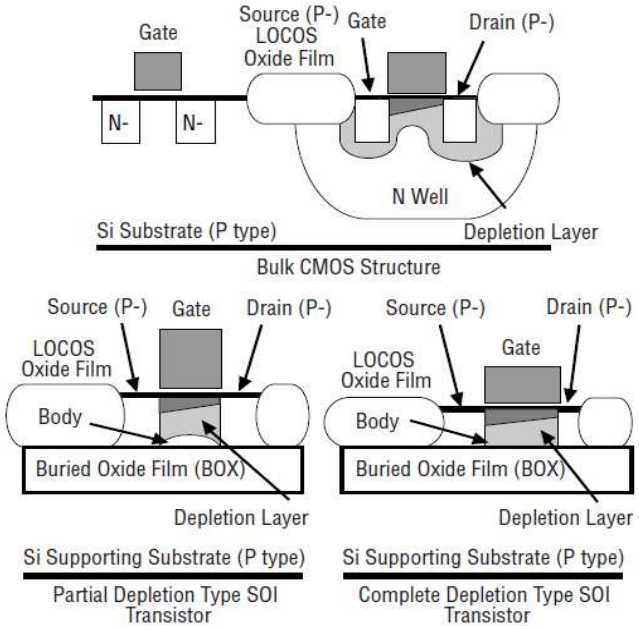

Figure 1: Comparison between bulk CMOS and SOI CMOS [2]

The most popular microelectronics technology is based on the conventional bulk CMOS structure where the device is placed directly on a bulk silicon substrate. Bulk CMOS devices however suffer from large parasitic capacitances and pronounced short channel effects because of the bulk silicon. An additional issue of BULK CMOS is caused by latch-up due to the n-well or p-well structure used to isolate the device, which may actually lead to a short circuit between n-channel and p-channel devices.

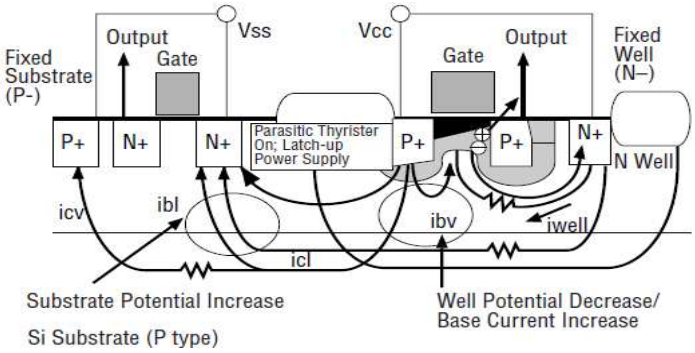

Figure 2: Latch up phenomenon of Bulk CMOS [2]

These issues are substantially minimized with the introduction of SOI technology whose n-channel MOSFET structure is shown in Figure 1. Unlike the conventional MOSFET technology, a layer of buried oxide (BOX) is placed between the thin silicon island, where the active device is, and the silicon substrate, as illustrated in Figure 1. The BOX layer effectively reduces the parasitic capacitance, diminishes short channel effects and resolves the latch-up issues in the conventional CMOS technology.

In SOI technology, the isolation of the device from the bulk substrate is the key in solving the problems faced by the bulk CMOS devices. This gives (SOI) CMOS structures numerous advantages over bulk CMOS, such as smaller leakage current, steeper sub-threshold slope, higher packing density, weaker short

channel effects, and smaller parasitic capacitances, etc [3]. The BOX in SOI however introduces a thermal barrier that enhances self-heating effects because of the low thermal conductive oxide. As a result, the average device temperature is substantially raised. In addition, due to the thin silicon island used as the active device region, large temperature gradients are observed in the silicon island and high peak junction temperature is induced. These reduce carrier saturation velocity and mobility and degrade device reliability and electronic characteristics. The higher device temperature also leads to stronger heat flow to interconnects and higher interconnect temperature, which increases the interconnect failure rate, delay time, joule heating and power consumption, etc [4].

3. The Fin FET Technology

With the SOI CMOS transistor channel length currently being below 25nm [5], the undesirable short channel effects present themselves as extremely detrimental issues. One of the solutions to these short channel effects comes in the form of 3 dimensional SOI CMOS structures. One of the leading novel types of these devices is known as FinFET technology, which is shown in Figure 3. The device channel is the middle part of the fin that is wrapped by the gate, which is a type of Tri-gated MOSFET. The fin under the gate is lightly doped. The rest of the silicon is doped with opposite polarity similar to a planar MOS. The smallest FinFET device dimensions we have found in the published literatures include a 10 nm gate length, and 12 nm fin width [6]. In FinFET devices, electrical potential throughout the channel is controlled by the gate-to-source and drain-to-source voltages. This is possible due to the proximity of gate control electrode to the current conduction path between source and drain. These characteristics of the FinFET minimize the short channel effect. Conventional MOSFET manufacturing processes can also be used to fabricate FinFET. They provide better area efficiency, and the mobility of the carriers can be improved by using FinFET process in conjunction with the strained silicon process [6].

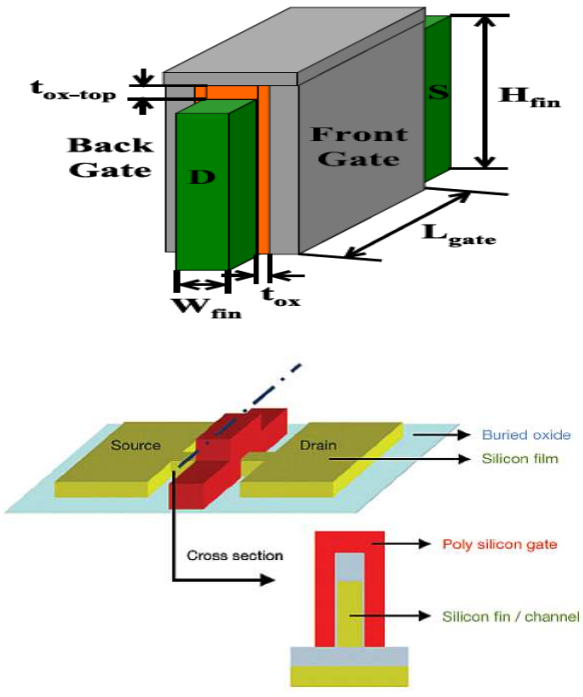

Figure 3: FinFET Device

3.1 Limitations of FinFET

Even though FinFET devices are seen as the leading solution to CMOS scaling limitations beyond the 22 nm node due to their superior electrostatics, thermal management in these ultra-scaled structures is an increasing concern. The issue of heating is made worse due to materials with poor thermal conductivity and the physical confinement of the device geometries lead to increased self-heating resulting in performance and reliability degradation. As FinFET process technology and integration progresses rapidly, FinFET parameters are being optimized to maximize their performance. It is necessary to simultaneously develop accurate and fast electro thermal modeling and simulation capability for simultaneous evaluation of the impact of the thermal characteristics on these parameters, which in turn impact the reliability and electrical performance of FinFETs. Self-heating is already known to degrade the drain current in SOI and strained-Si devices by around 15% due to the presence of a BOX in SOI type devices or a SiGe graded layer in strained-Si devices that increases the thermal resistance of the device due to low thermal conductivity of these materials [6,7]. In FinFETs, the problem increases manifolds due to the small and confined dimensions of the fin that reduce its thermal conductivity. Self-heating is also known to degrade oxide reliability of FinFET devices [8,9].

4. Proposed Thermal Circuit Model for Fin FET

The proposed thesis work includes development of a thermal circuit for FinFET structure, accounting for non-isothermal effects along the fin, and implementation of the thermal circuit in a circuit simulator, such as Spice, for efficient and accurate electro-thermal simulation. Eventually, the electro-thermal simulation of FinFETs will be performed, and the thermal solution will be validated against finite element simulation.

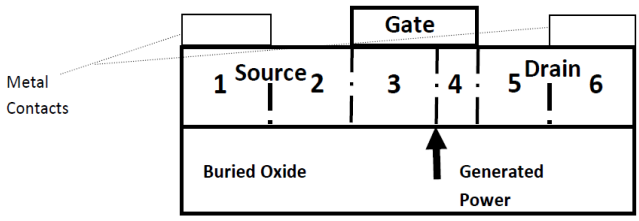

Figure 4: Proposed Fin FET model

Figure shows a 2-D cross section of the FinFET from the source via the channel to the drain. The dash lines divide the film into six uniform regions for constructing the thermal circuit. The gate is supposed to wrap 3 sides of the channel, including top, front and back sides, as illustrated in Figure 3. For clarification of region divisions, only the top gate is shown.

4.1 Heat flow along the source, drain and fin

The first step requires solving the analytical thermal solution in each region on the silicon island, including the active device regions wrapped by the gate, the fin regions between the source/drain and the channel, and the source and drain contact regions. The metal contact on top of the large source/drain region shown in Figure 4 is not included in Figure 3. The heat flow along the silicon island needs to be determined, which will provide the accurate thermal profile along the island. The profile is needed to provide more accurate heat flow to the interconnects and the poly gate, which is crucial for prediction of interconnect temperature and thermal coupling between nearby devices. The analytical solution will then be converted into thermal circuit for the FinFETs. Implementation of the thermal circuit will allow channel temperature coupled with electrical model of the FinFET for self-consistent electro-thermal simulation. Similar to [10,11], in order to model the heat flow through the FinFET, the island is divided into uniform regions as shown in Figure 4. To account for the generated power, which is located in the channel-drain junction, the island is divided such that the power input is at the channel-drain junction which is the division boundary of Regions 3 and

4. The temperature of the portions of the source and drain regions under the metal contacts (Regions 1 and 6) can be assumed to be approximately constant because metal has a very high thermal conductivity. Therefore it is only necessary to solve the heat equation in 4 regions; i.e., Regions 2-5 shown in Figure 4. Regions 1 and 6 can then be taken as thermal nodes. Once the uniform regions are selected in the FinFET device, 2 boundary conditions (BC's) for each interface between adjacent regions are needed to obtain analytical solution, including temperature and heat flux continuities at the interface. The analogy of these BC's is the voltage and current continuities at the node that connects the circuit elements. This may include a current source that provides a current flowing into the node. The analogy is explained in detail in [11]. This is similar to a power source in the thermal flow problem, such as the generated power at the interface between Regions 3 and 4 in Figure 4. Because of the thin island structure, temperature vertical to the island surface can be assumed constant. Also, due to the uniform power generation along the device width direction, the problem of heat flow along the thin island is reduced to a 1D problem if the heat flow out of the island is treated as losses that can be described by constant characteristic thermal lengths due to different heat loss paths. To obtain the accurate temperature profile, a detailed numerical simulation is usually necessary. In this project, the thermal lengths will be studied and determined in terms of thermal resistances of the SOI structure and its terminals that will be extracted from a finite element simulation.

5. Conclusion

Although detailed numerical is able to offer accurate temperature profiles in devices to capture the device peak temperatures, any numerical simulation of FinFETs, including the finite element method, is very time consuming. As accurate as finite element simulations are, they become very impractical once we consider any common integrated circuits which require hundreds of thousands of transistors. In order to design any integrated circuit using the electrical model of devices, the information about the influence of its heating on electrical characteristics is very important. The proposed thermal circuit model is able to provide detailed heating information on FinFETs efficiently and accurate, and will offer an effective electro-thermal simulation tool for cost effective FinFET chip design.

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