Industrial Engineering Letters
ISSN 2224-6096 (Paper) ISSN 2225-0581 (online)
Vol.5, No.6, 2015

Designing of Different High Efficiency Diode Clamped Multilevel Inverters and their Performance Analysis

Mubarak Ahmad[1], Javed Ali Khan[2], Hashim Khan[3], Mian Izaz ur Rehman[4], Yawar Hayat[5], Liaqat Ali[6]
[1]Department of Electrical Engineering CECOS University Peshawar, Pakistan
[2,3,4]Department of Software Engineering University of Science and Technology Bannu, Pakistan
[5]School of Information Technology University of Lahore Islamabad, Pakistan
[6]Department of Electrical Engineering University of Science and Technology Bannu, Pakistan

Abstract

This research work is aimed at designing of high efficiency multilevel diode clamped inverter. It would cover diode clamped multilevel inverter with particular reference to the comparison of high level and low level inverter using efficient modulation method (sinusoidal pulse width modulation). The main theme of this research is to obtain a pure sinusoidal waveform of high quality having minimum harmonics that can be utilized for both industrial purposes and to sensitive domestic loads. The proposed design besides considering high quality of the output waveform of multilevel diode clamped inverter, the problems regarding multilevel inverter design has been given more consideration high voltage stresses across switching devices. The voltage stresses issues have been resolved with DC link voltage equally distributed among capacitors in multilevel inverter. Simulation results for different level inverters both low level (5, 7, 9, level) and high levels (11, 13, 15) are used as a reference. The proposed design resulted in reduced total harmonic distortion thus eliminating the harmonics in the output waveform to a greater extent resulting in pure sine waveform output. This resulted in reduction in overall losses and elimination of voltage balancing problems in high level diode clamped inverter.

Keywords: Hormonics, Clamping, Inverter, Pulse Width Modulation, Sinusoidal Pulse Width Modulation (SPWM).

1.Introduction

The main objective of this research work is to perform the simulation of three phase (nine, eleven and thirteen) level diode clamped inverter by using the technique of sinusoidal pulse width modulation for getting the output waveform of good quality, better efficiency resembling with the sinusoidal waveform and of low cost. A comparison between the different level inverters is also made. The comparison results will show that how much improvement can be obtained with the change in the number of levels. The main work is focused on DC link utilization, improved output waveform and the issues regarding balancing of capacitor voltages.

The whole research work can be categorized as

- Designing of three phase multilevel diode clamped inverter circuitry.
- Utilization of precise modulation technique for the proper operation of multilevel diode clamped inverter.
- To use Simulink for the design of controlling circuit.
- Designing of filter to obtain the pure sinusoidal waveform.
- Judgment of diode clamped inverters of low level and high level.

2. Literature Survey

The main issue regarding multilevel diode clamped inverter is of the balancing of capacitor voltage at the input side that increases with increase in increasing the number of levels in the inverter. The same dc link capacitors are used for three phase operation so balancing problem effect all three phases. As the number of levels increases the balancing of the voltage becomes more complicated. Proper design strategies should be planned to overcome this balancing problem. Different researches presented different approaches to overcome this problem.

[1] Newton et al. (1997) proposed an approach of utilization of a small DC offset to the modulating signal to manage the balance by voltage. This approach is only applicable to three phase systems where the DC offset

voltage cancels each other at the line to line voltages. As a result the three phase load currents are free from the DC offset value.

[2] Newton et al. (1998) used another approach of auxiliary balancing circuitry to overcome the voltage balancing problem between the DC link capacitors. The proposed method is three level and five level inverters. However its main limitations are losses, complexity of the circuitry and high cost.

[3] Pou (2005) and Maryam. S et al. (2007) gave a concept of redundant state values of space vector modulation technique that has the same line voltage but of opposite effect on DC link capacitors. However with the increase in the number of levels the usable redundant states which cause voltage balancing tends to occur at the middle of the space vector topology. This shows the modulation index to be in the limit, gives low harmonic concert causing this approach unrealistic.

[4] Adam.Grain P et al. (2012) gave the concept of Quasi 2 level operation for five level diode clamped inverter to solve the issue of capacitor balancing. The maximum attained modulation index for Quasi 2 level inverter is .937 using SPWM technique maintaining unity power factor. This research has also achieved some key objectives like reduction in DC link capacitor size and development in DC link voltage consumption for more than three level diode clamped inverters.

[5] Adam et al (2010) worked more on Quasi 2 level operation using SPWM for the diode clamped multilevel inverter. This research work was confirmed experimentally using five level diode clamped inverter to extend the modulation index linearly.

[6] Zhiguo pan et al (2005) gave a new approach of voltage balancing control for diode-clamped multilevel inverter. A complete analysis of voltage balance theory for a five-level back to back system is being presented. The projected control approach regulates the dc bus voltage, balances the capacitors, and causes to decrease harmonic contents of the voltage and current.

[7] Arash et al. (2010) presented a new single-inductor multi-output dc/dc converter for the controlling of dc-link voltages of a single-phase diode-clamped inverter asymmetrically to achieve voltage quality improvement. The circuit of the existing converter is explained and the main equations are developed.

3. Proposed Mechanisms and their Comparisions

Multilevel inverters are being operated at low frequencies. The low frequency operation reduces switching losses, which is the main advantage of multilevel power inverters. Multilevel inverters are applicable for medium and high voltage applications. The main disadvantage of multilevel inverter is its high complex circuitry and high number of switches. Different types of inverters are used like diode clamped inverters, flying capacitors and cascaded inverters.

3.1 Nine Level Inverter

3.1.1 Leg Voltages and Line Output Voltages of Nine Level Inverter

For the three phase 9 level diode clamped inverter, each leg has sixteen clamping diodes. Three phase 9 level diode clamped inverter has different switching states which produces nine voltage levels.

Line output voltages are as under

$V_{ab}(t) = V_{an}(t) - V_{bn}(t)$..... (1)

$V_{bc}(t) = V_{bn}(t) - V_{cn}(t)$..... (2)

$V_{ca}(t) = V_{cn}(t) - V_{an}(t)$..... (3)

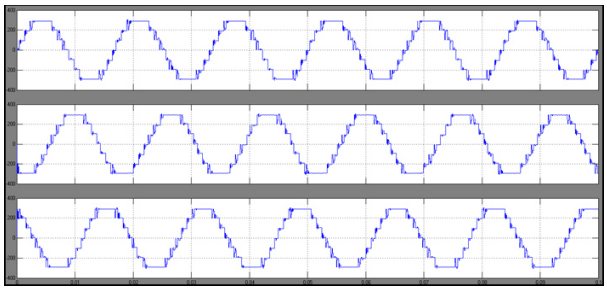

Figure 1 Leg Voltages of Three Phase Nine Level Inverter

Where V_{an}, V_{bn} and V_{cn} represents phase voltages and V_{ab}, V_{bc} and V_{ca} are line voltages respectively shown in figure

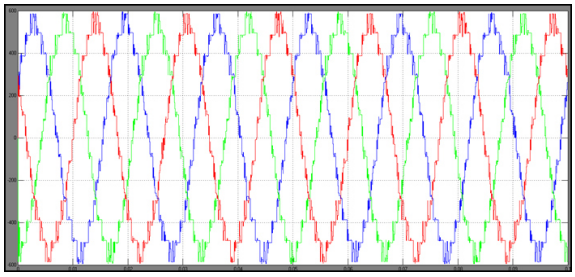

Figure 2 Line Voltages (Unfiltered) of three phase Nine Level Diode Clamped Inverter

The staircase waveform is generated by different states of the power switches containing redundant, non adjacent and adjacent states. Some switching states produce same voltage level for each of line voltage, called redundant states. The line voltage in staircase waveform resembles sinusoidal waveform. Line voltages having harmonic contents are passed through filter to obtain pure sinusoidal waveform. Filtered voltages are shown in figure 3.

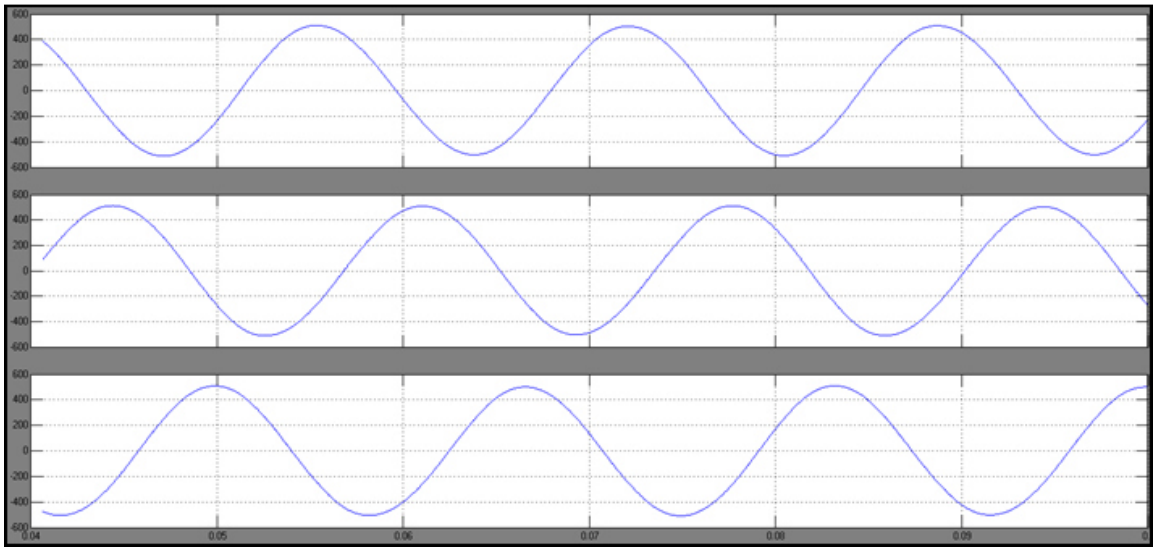

Figure 3 Filtered Line Output Voltages of Three Phase Nine Level Inverter

3.1.2 Nine Level Diode Clamped Inverter (SPWM) control

In nine level diode clamped inverter output voltage reaches to high value having low contents of harmonic distortion. Diode clamped inverter uses diodes in series connection to reduce or limit voltage stresses on switches. Calculation of capacitors for n-level diode clamped inverter is like [n-1] capacitors, 2[n-1] power

switches and [n-1][n-2] diodes for clamping. Using above calculation eleven level diode clamped inverter has 10 capacitors, 20 power semiconductor switches and 90 clamping diodes.

3.2 Eleven Level Inverter

3.2.1 Eleven Levels Voltage

Each leg of three phase, eleven level diode clamped inverter is highlighted in figure (2.6), where C_1, C_2, C_3…C_{10} represents DC link capacitors and S_1, S_2, S_3……..S_{20} are power switching devices of Gate Turn Off Thyristor (GTO).

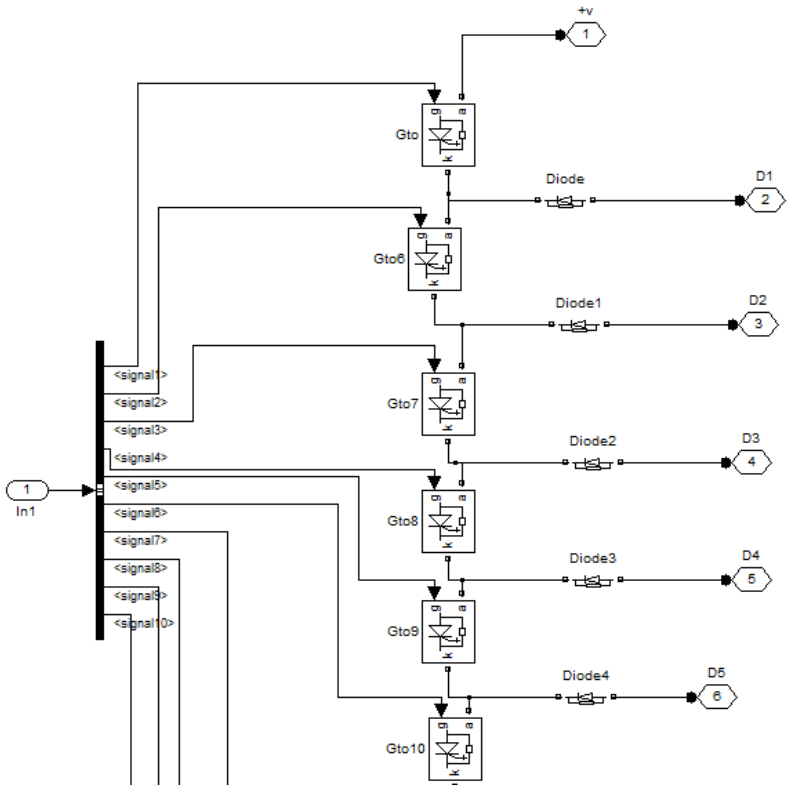

Figure 4 Leg structure of Inverter

To generate different levels/steps at output side of an eleven level/steps diode clamped inverter 10 power switches will be conducting at every instant at once. The Simulink execution of three phase, 11 level inverter is shown as under

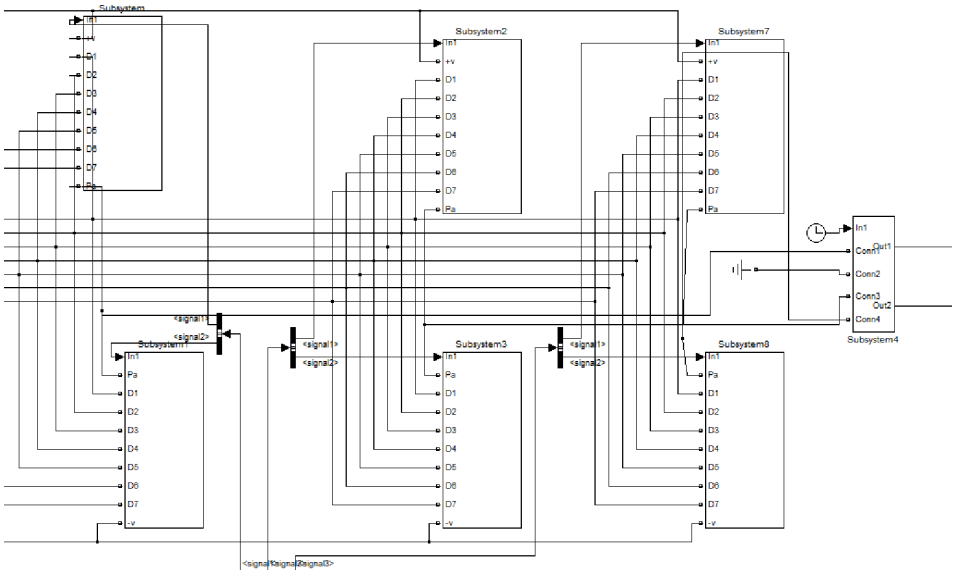

Figure 5 Simulink Implementation of the Inverter

3.2.2 Leg/Phase Voltages

Three phase eleven level diode clamped inverter shows eighteen clamping diodes and ten power switching components (GTOs). Every leg voltage has eleven different voltage levels/steps in the stair case pattern shown as in figure 6.

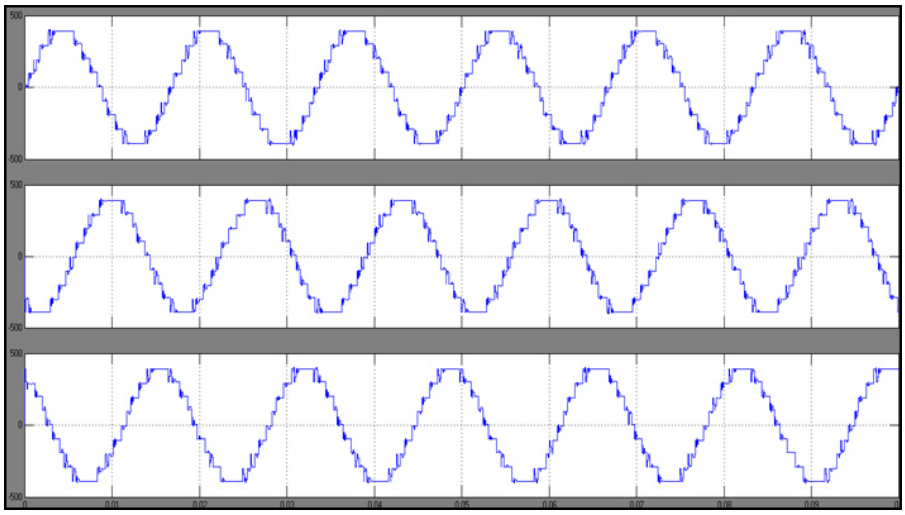

Figure 6 Leg Voltages of three phase eleven level diode clamped inverter

Figure 6 shows that each leg voltage has eleven different voltage levels. Similarly other two voltage legs are shown similar in construction with different voltage levels. These voltage legs are phase voltages denoted by $V_{an}(t)$, $V_{bn}(t)$, $V_{cn}(t)$ respectively.

3.2.3 Line Output Voltages of 11 Level Diode Clamped Inverter

Line voltages are obtained in the following pattern

$$V_{ab}(t) = V_{an}(t) - V_{bn}(t) \quad \text{(4)}$$

$$V_{bc}(t) = V_{bn}(t) - V_{cn}(t) \quad \text{(5)}$$

$$V_{ca}(t) = V_{cn}(t) - V_{an}(t) \quad \text{(6)}$$

These voltages are presented in below figure 7.

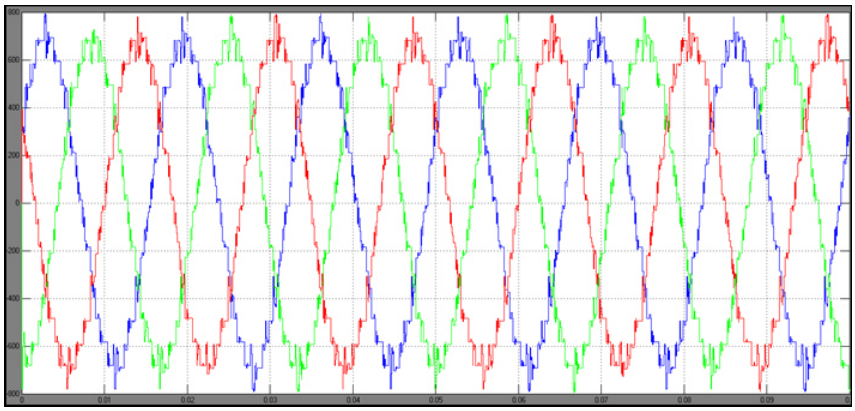

Figure 7 Three phase eleven level diode clamped inverter line voltages

3.2.4 Sinusoidal Output Line Voltage (Filtered Output)

For improvement in output voltage efficiency and performance ability of the three phase eleven level diode clamped inverter, it is needed to generate output line voltage with least amount of harmonic contents. Different methods are employed to lower harmonic contents from unfiltered output line voltages. Which are,

1. Proper selection of angles for switching devices.
2. Increasing number of voltage levels.
3. Using filter circuit.

Proper and accurate calculation of switching angles for each switch ensures harmonic elimination to a greater extent and results in pure output voltage.

Increasing number of voltage levels results in reduction of harmonic contents in the output. In this method increasing of number of steps minimizes the total harmonic distortion. Total harmonic distortion decreases by increasing number of DC link capacitors. This whole arrangement causes to increase the complexity of system and cost.

The output waveform contains harmonic contents, which are eliminated by using low pass filter. The filtered line voltages are shown in figure 8.

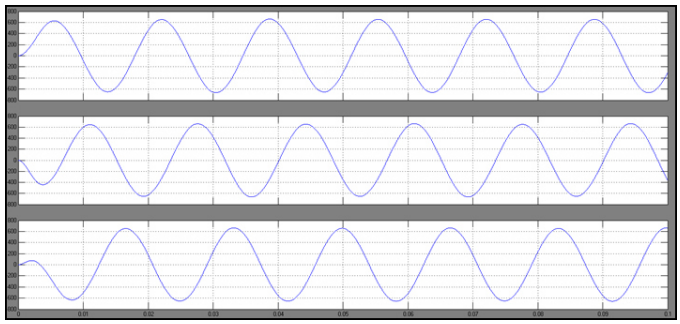

Figure 8 Line Voltages of 3-Phase 11-Level Diode Clamped Inverter (Filtered Output)

3.3 Summary of Design of Nine Level & Eleven Level Inverters

In the above sections i.e 3.1 and 3.2 we discussed the design of three phase nine level and eleven level diode clamped inverter using Simulink. Simulink model gives graphical representation of three phase nine level and three phase eleven level diode clamped inverters whose output is in staircase waveform resembling sinusoidal output waveform. The staircase waveform is due to DC link capacitors. Harmonic contents in output waveform of the unfiltered circuit are eliminated by filter.

3.4 Thirteen Level Diode Clamped Inverter

Thirteen level diode clamped inverter compared with low level (3 or 5 levels) inverters has an advantage that it can use DC voltage sources in input for generation of multilevel output.

High level (thirteen levels) inverter has high level used for high voltage applications. Low level inverters have MOSFETS as their switching devices, but MOSFETS are not used because of low efficiency for high power applications and high voltages. MOSFETS have 2V of forward voltage drop which generates voltage losses in the switching devices of the diode clamped multilevel inverter. MOSFETS have the capability of low power handling of less than 10KVA, 1000V, 200 A due to forward voltage drop. MOSFETS are not used in high level diode clamped inverters.

To minimize the switching losses Gate Turn Off Thyristor (GTO) are used as switching device. This high level (thirteen) inverter is more proficient as compared to low level inverter as the output of (thirteen) high level inverter has less amount of harmonic contents. The input of this thirteen level inverter has high number of DC voltage sources. This high number of DC sources causes reduction of harmonics. The Simulink design of thirteen level inverter is given as under

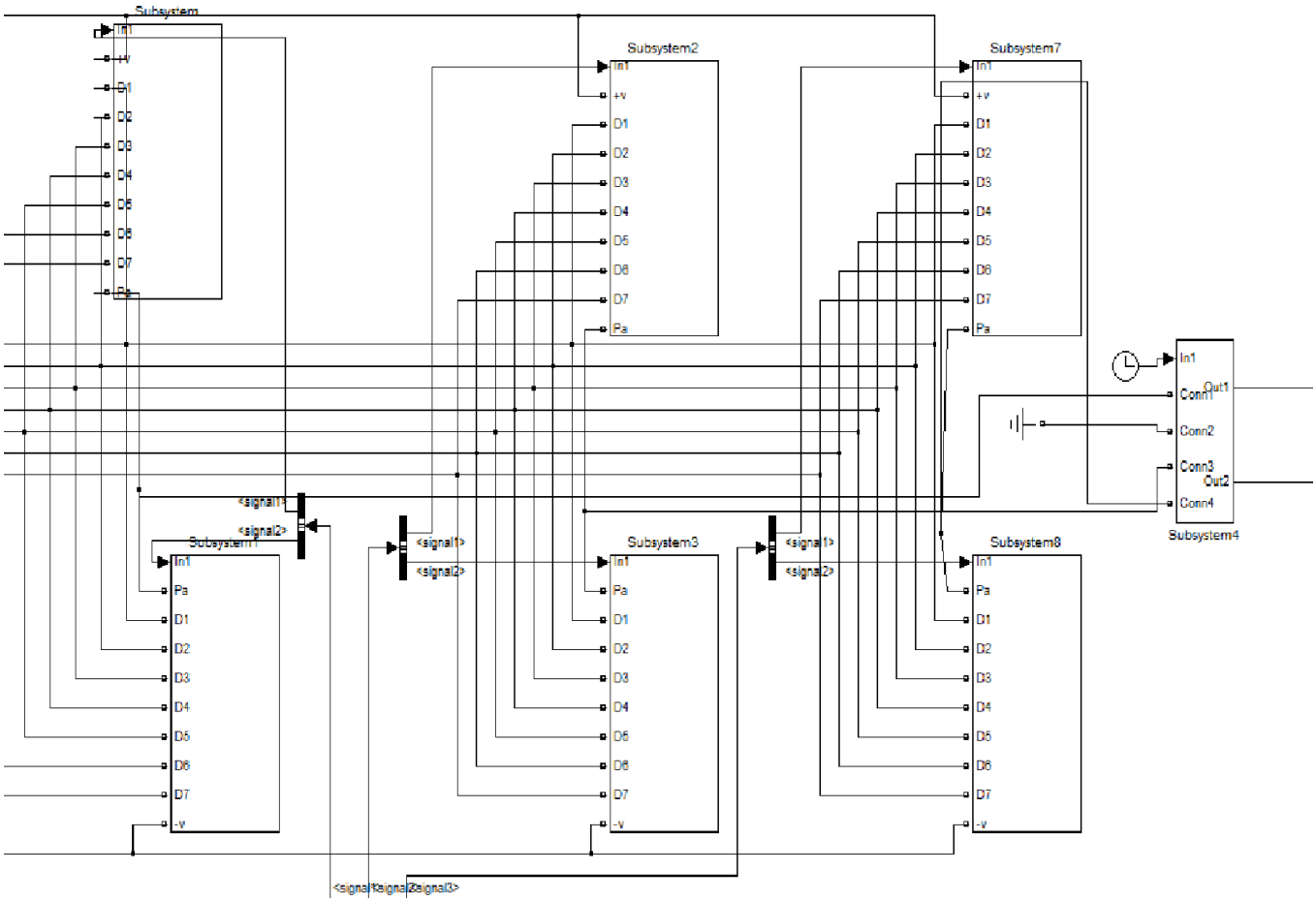

Figure 9 Simulink design of the 13 level diode clamped inverter

Above are the modules labeled as subsystem, subsystem1, subsystem2, subsystem3, subsystem4, subsystem5. Every module has an internal structure of series connected GTO's and clamping diodes for switching of high power and high voltage handling capability. The clamping diodes are used to reduce the abnormal voltage stresses across GTO's and protect the circuit from damaging. GTO's switch is a full controlled switch which can be switched ON by giving a +ve gate pulse and turned OFF by providing the –ve gate pulse. The GTO's has high voltage (up to 6KV) and high current (up to 6A) ratings are favorable for high voltage and high current applications.

Each subsystem has (n-1) Gate Turn Off Thyristor as shown. Where n is the number of levels.

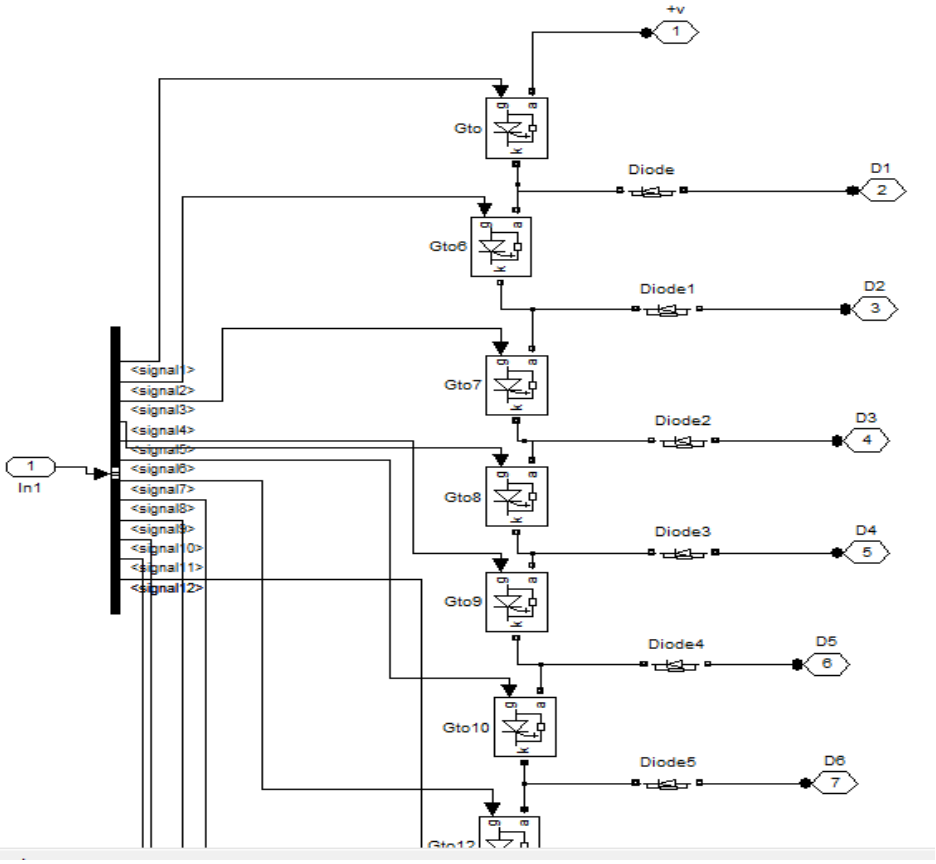

Figure 10 Internal structure of the Subsystem Module

Subsystem 6 has an important role for proper operation of switching devices. This system provides control signals for GTO‘s. Gate pulses are generated by comparing the reference and carrier signals.

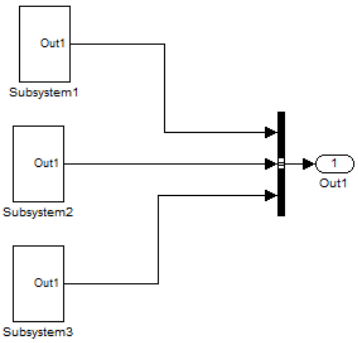

Figure 11 Internal structure of the subsystem 6

Output of mux/bus selector is then given to blocks as input signal. Output signal is subdivided into three signals known as signal1, signal2 and signal3. The signal1 is further subdivided in two signals by using a bus selector and labeled as signal1, signal2. Each sub signal consists of (N-1) gate pulses (obtained by proper selection of modulation technique) used for controlling of power switches. The sub signal is given to subsystem for controlling purposes. Similarly subsignal2 is given to subsystem1 for controlling as described for sub signal1. The remaining two signals of bus creator are given to other four modules/subsystems for the same controlling function. The detail of the six control signals is shown in figure 12

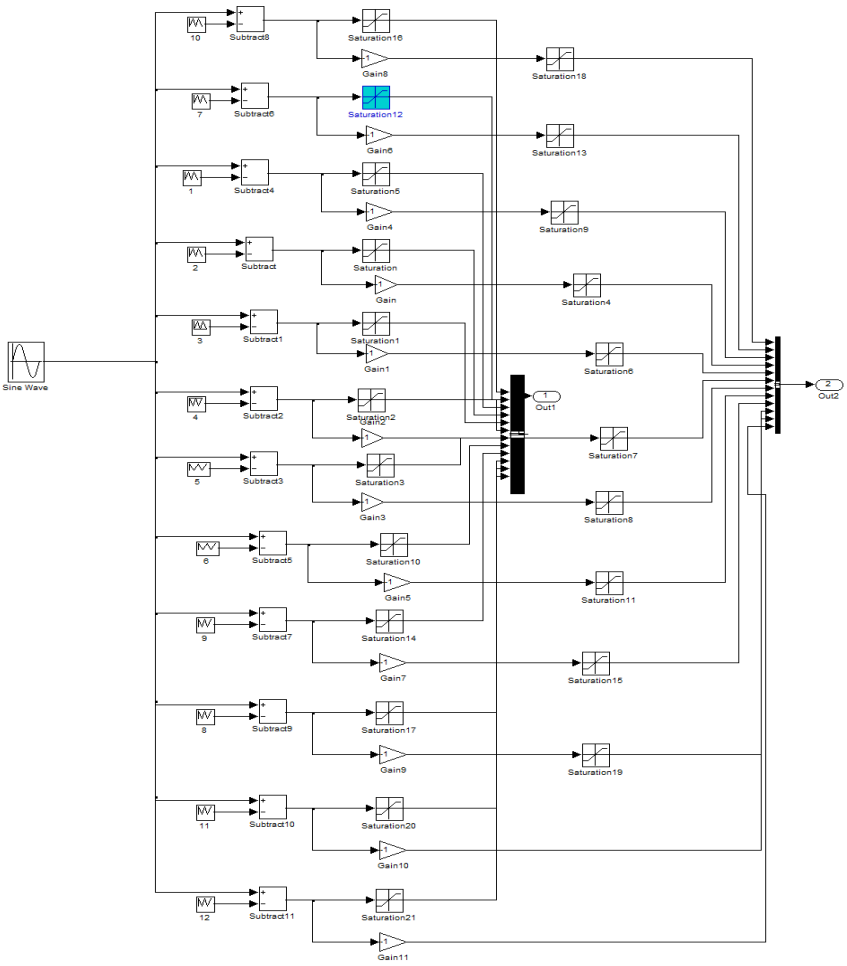

Figure 12 Control pulses for GTO's

The bus selector has three output signals and one input signal. These output signals are used to control the six modules/subsystems for proper operation of semi conductor devices.

3.4.1 Output line voltages

The output line voltages can be fined out in the following way

$V_{ab}(t) = V_{an}(t) - V_{bn}(t)$..... (7)

$V_{bc}(t) = V_{bn}(t) - V_{cn}(t)$..... (8)

$V_{ca}(t) = V_{cn}(t) - V_{an}(t)$..... (9)

These voltage waveforms are shown as

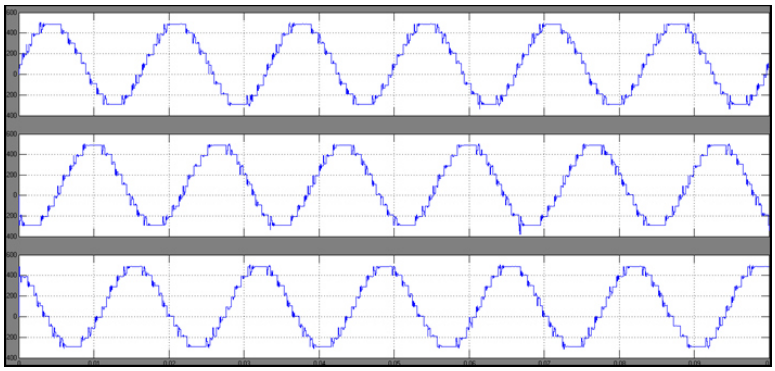

Figure 13 Line Voltages (Unfiltered)

3.4.2 Sinusoidal Output (Filtered Output)

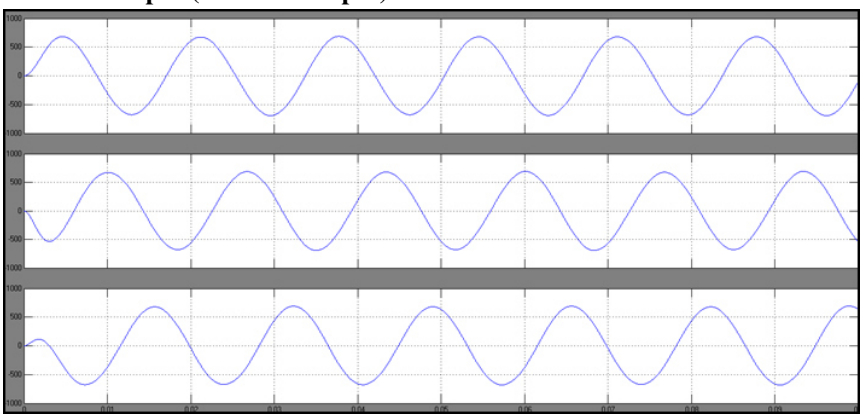

Figure 14 Line Output Voltage (Filtered Output)

3.4.3 Summary of Design of Thirteen Level Inverter

The section 3.4 discussed the Simulink design of thirteen level diode clamped multilevel inverter. Thirteen level inverter has advantage over low level diode clamped multilevel inverter like reduction in harmonic contents and producing more efficient and good quality sinusoidal output waveform. Thirteen level diode clamped inverter has more number of GTO's or switching devices to achieve thirteen levels in output waveform. It has an advantage of using less costly and small filters. It increases the cost and complexity of the overall system.

4. Comparison of low and high level inverters

4.1 Comparison between low and high level diode clamped multilevel inverter

Comparison between three phase nine level, three phase eleven level and three phase thirteen level diode clamped inverter is presented. There are different features describing difference between low and high level inverters.

4.1.1 Structural difference

Low level (three phase five level) and high level (nine level three phase, eleven level three phase) inverters have three legs parallel to each other. Each leg has its own staircase voltage waveform. Both types of inverters have switching devices e.g MOSFET's, IGBT's, GTO's depending upon number of levels. As number of levels increases number of switching devices also increases. Besides it has anti parallel and clamping diodes in each leg.

4.1.2 Different output voltages

Both low level (five level three phase) and high level (three phase nine level, three phase eleven level and three phase thirteen level) inverters have staircase output waveforms which can be differentiated by the number of levels. Three phase five level, three phase nine level and three phase eleven level diode clamped inverters have five, nine and eleven levels respectively in its output waveform.

4.1.3 Total harmonic contents

Total Harmonic contents of nine level inverter are much lower than low level inverters. Harmonic contents depend upon the number of levels in the output waveform. Increasing number of levels or steps decreases THD. Increasing number of voltage levels results in waveform close to sinusoidal waveform.

The FFT window shows complete data information about THD in low level diode clamped inverter (five level inverter) where total harmonic distortion is 20.56% as shown in figure 15.

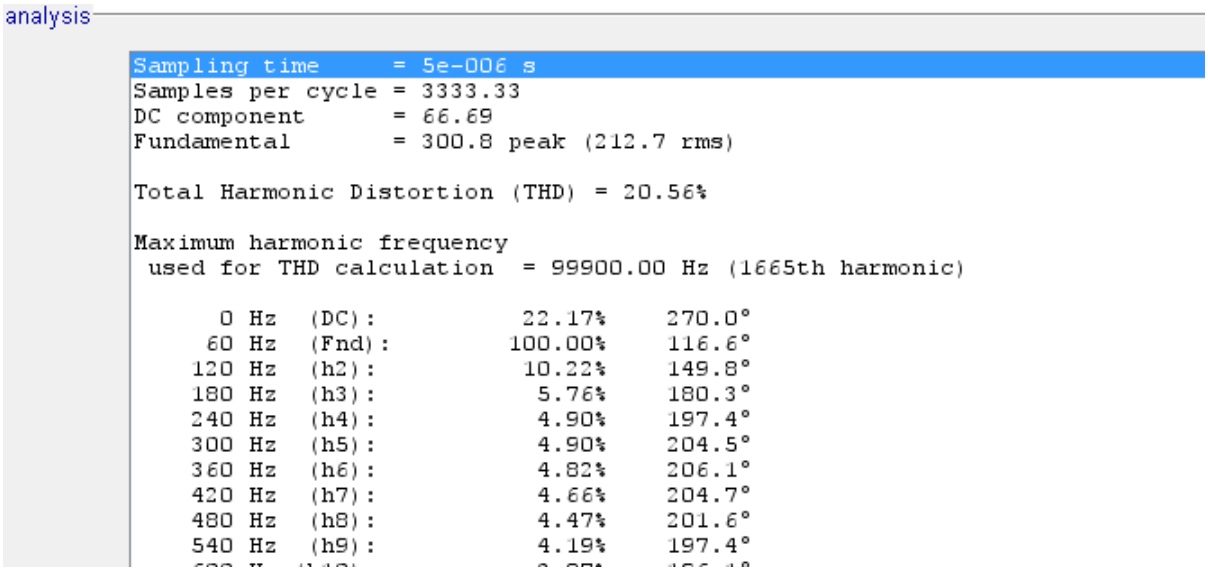

Figure 15 FFT window for 5 Level Diode Clamped Inverter

Similarly the total harmonic distortion for high level (eleven level) diode clamped inverter is shown which has the value 5.68% as shown in the figure 16.

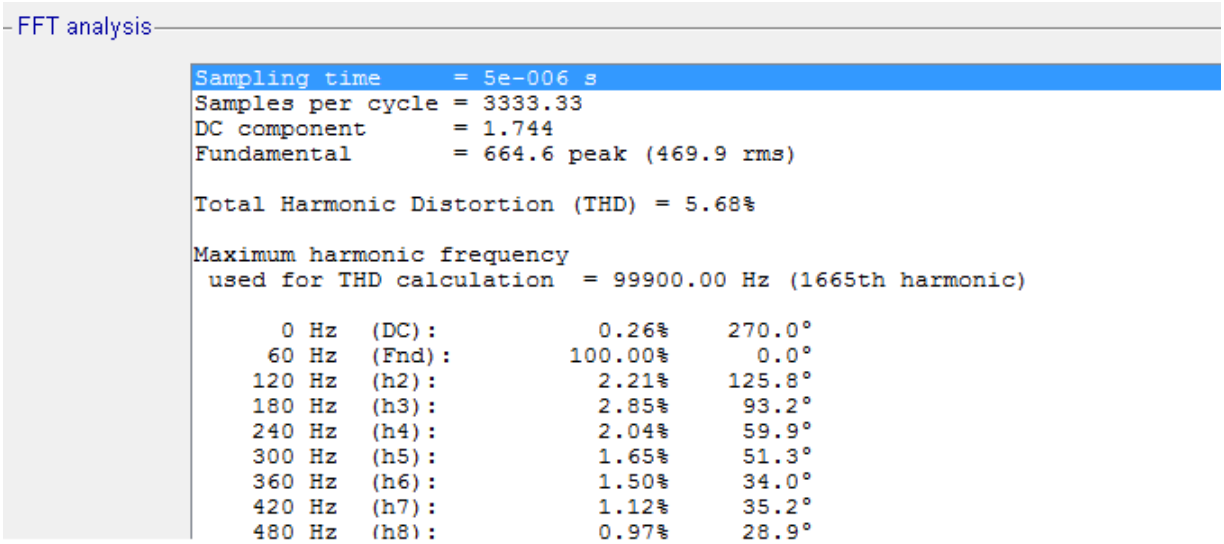

Figure 16 FFT window for 11 Level Diode Clamped Inverter

Similarly the total harmonic distortion for high level (thirteen level) diode clamped inverter is shown which has the value 4.49% as shown in figure 17.

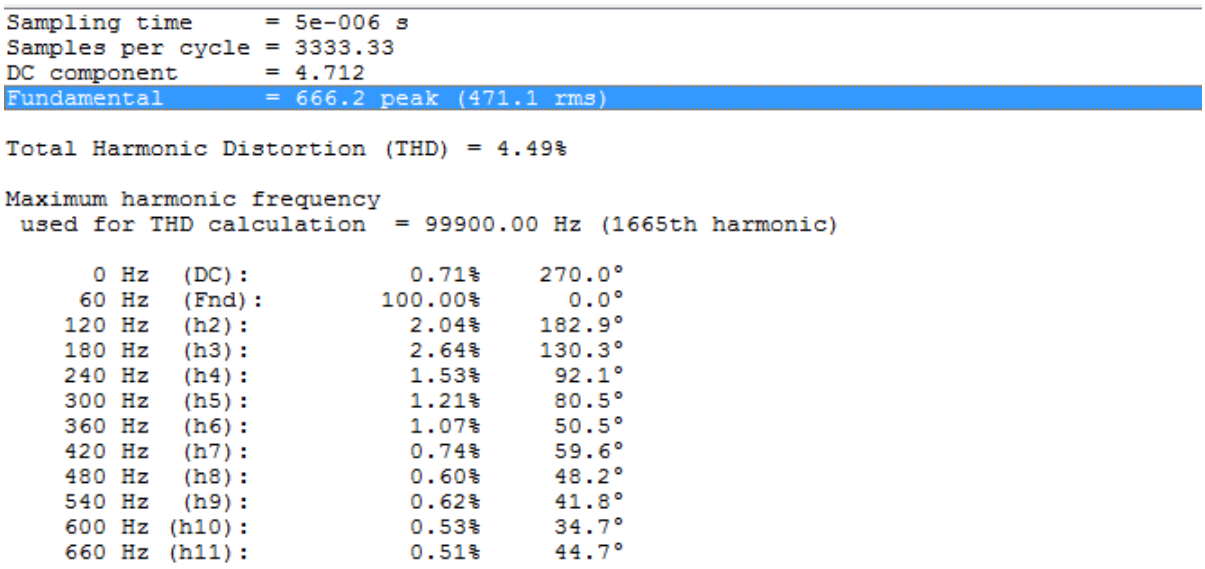

Figure 17 FFT window for 13 Level Diode Clamped Inverter

The figure shows that if number of levels/steps in output increases then THD decreases.

5. Conclusion and Future Work

A comparison is made between low and high level diode clamped inverter. The comparison shows certain features of low and high level diode clamped inverters like structural comparison, comparison between numbers of levels/steps. Decreasing THD was observed by Fast Fourier Transform (FFT) analysis.

Multilevel diode clamped inverters are widely used for medium and high power applications due to its special structural design. In multilevel inverters the improvement of voltage quality and reduction of voltage stresses upon switching components are the main achievements. Besides these advantages, there are some serious issues regarding balancing of DC link capacitors voltage in diode clamped inverters. These issues if not properly cared can cause dangerous to switching components and produce large number of harmonics in output.

The main advantage of multilevel diode clamped inverter topology is the accomplishment in large number of DC voltage levels at the output possible by placing large number of electronic components. The treatment of large number of equipments causes complexity of the overall system. Increasing complexity of the system increases cost of the system. Besides these issues multilevel diode clamped inverter has attained an unavoidable place in industrial application as well as in renewable power sources.

This research effort has got development regarding quality of the output voltage, hence still more research work is required to improve the efficiency of overall system. To get rid of the problems of DC voltage balancing more work is required.

As multilevel inverters are mostly the requirement of industrial applications so we need a fault diagnose system designing to detect the fault and correct it to give safety to the remaining system. The diagnose system should has the ability of detecting the fault point, location and type of fault and efficient utilization of this inverter topology without interrupting the rest of system.

References

1. Arash A. Boora, Alireza Nami, Firuz Zare,Arindam Ghosh, and Frede Blaabjerg, 2010 Voltage-Sharing Converter to Supply Single-Phase Asymmetrical Four-Level Diode-Clamped Inverter With High Power Factor Loads, IEEE Trans On Power Electronics, 25: 10. 2507-2520.

2. Grain P. Adam, Stephen J. Finney, Ahmed M. Massoud, and Barry W. Williams, 2008 Capacitor Balance Issues of the Diode-Clamped International Journal of Reviews in Computing 31stJuly 2012.Vol. 10© 2009 -

2012 IJRIC & LLS. All rights reserved ISSN: 2076-3328 www.ijric.org E-ISSN: 2076-333612IJRIC Multilevel Inverter Operated in a Quasi Two-State Mode IEEE Trans on Industrial Electronics, 55:8.3088- 3099.

3. Adam. Grain P. et al. 2010. Two-Level operation of a diode clamped multilevel inverter. IEEE Trans.

4. Attaianese, M. and G. Tomasso, 2010 Three-Phase Three-Level Active NPC Converters for High Power System, International Symposium on Power Electronics, Electrical Drives, Automation and Motion, 204-209, Speedam.

5. G.Bhuvaneshwari and Nagaraju Multilevel inverters – a comparative study, 51:2 march – april 2005.

6. Janyavula Deepthi and Saxena, S.N. (2011), Study of Variation of THD in a Diode Clamped Multilevel Inverter with respect to Modulation Index and Control Strategy, 2nd International Conference and workshop on Emerging Trends in Technology (ICWET) , 51:7.37-42.

7. Jing Huang and Corzine, K.A. (2006), Extended Operation of Flying Capacitor Multilevel Inverters, IEEE Trans. on Power Electronics, 21: 1.140-147.

The IISTE is a pioneer in the Open-Access hosting service and academic event management. The aim of the firm is Accelerating Global Knowledge Sharing.

More information about the firm can be found on the homepage:
http://www.iiste.org

CALL FOR JOURNAL PAPERS

There are more than 30 peer-reviewed academic journals hosted under the hosting platform.

Prospective authors of journals can find the submission instruction on the following page: http://www.iiste.org/journals/ All the journals articles are available online to the readers all over the world without financial, legal, or technical barriers other than those inseparable from gaining access to the internet itself. Paper version of the journals is also available upon request of readers and authors.

MORE RESOURCES

Book publication information: http://www.iiste.org/book/

Academic conference: http://www.iiste.org/conference/upcoming-conferences-call-for-paper/

IISTE Knowledge Sharing Partners

EBSCO, Index Copernicus, Ulrich's Periodicals Directory, JournalTOCS, PKP Open Archives Harvester, Bielefeld Academic Search Engine, Elektronische Zeitschriftenbibliothek EZB, Open J-Gate, OCLC WorldCat, Universe Digtial Library , NewJour, Google Scholar