Control Theory and Informatics
ISSN 2224-5774 (print) ISSN 2225-0492 (online)
Vol 2, No.2, 2012

Optimizing the Output Current for a DC-DC Converter

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Abstract

Portable product design requires that power supply circuits use as little space as possible on the PC board, so highly integrated DC-DC converter devices are generally preferred. System designers need to understand the maximum amount of power that can be delivered by a given integrated circuit solution. Total output power capability is not only a function of the power converter IC, but also dependent on external components and operating frequency. This paper explores the relationship between a power converter's rated switch current and its effective load current capability for two common DC-DC converter topologies, the non-isolated buck and boost circuits. By proper selection of external components and operating frequency, it is possible to maximize the output current available from a given power conversion device.

Keywords: Converters, switching frequency, buck, boost, inductor, components, switch, current.

1. Introduction

Many integrated power converters are characterized according to their internal current limit capability. This is not unusual, since IC specifications can only define the capability of the silicon itself… the system designer, on the other hand, generally begins with the requirement for power needed for a system load outside of the chip.

In a traditional power supply design environment, the power switching elements are external to the power control device, and can be scaled as needed to meet the system load requirements. In a portable design with integrated power switches, the system designer is constrained to the internal switch current rating for the IC that is being used. In the case where a power converter does not quite seem to deliver the needed output current, the initial tendency may be to "choose a bigger part." In a space- and cost-sensitive environment, however, this may not always be the best approach.

The relationship between the current flowing in the power switches of a DC-DC converter (internal to the power IC) and the load (external to the power IC) can be determined based on the operating conditions and external component values in the circuit.

The maximum output current capability for the overall power supply depends on the switch current limit rating (silicon specification), the input-output voltage relationship (application specific requirement), the inductor value (external component selection), and switching frequency (determined by the choice of the IC or by external component values). These relationships are derived for the ideal converter, and also demonstrated through use of measured data from actual converter circuits under different load conditions.

2. Buck Converter

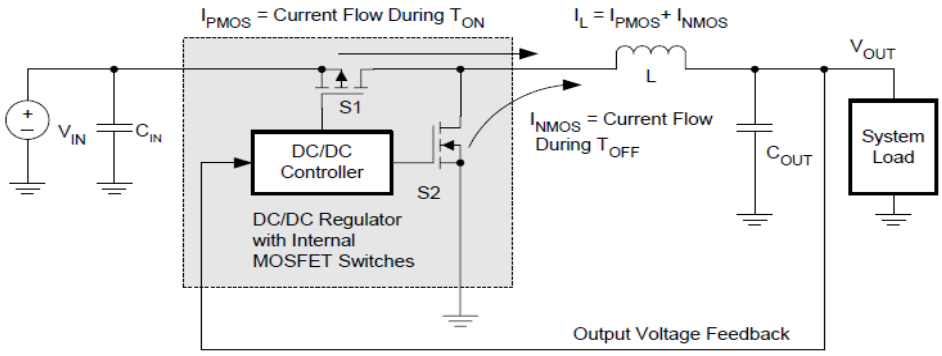


Figure 1. Simplified synchronous DC-DC buck converter.

Fig. 1 illustrates a simplified synchronous buck converter circuit with internal power switches. The illustration is typical of many portable DC-DC converter designs which use a PMOS high-side switch and an NMOS low-side (synchronous rectifier) switch. A traditional (non-synchronous) buck converter uses a diode in place of the NMOS switch, but the analysis for the ideal case is basically the same if switch or rectifier losses are ignored. The NMOS switch is turned ON only during the time that the PMOS switch is turned OFF. If the PMOS switch is ON, then the NMOS switch is OFF.

When loaded at a high current level, the converter operates in continuous conduction mode; in other words, there is always some amount of current flowing in the inductor. Assuming steady state operation, V_{OUT} is a constant (DC). Since the voltage across C_{OUT} is constant, the average capacitor current is zero, so the average current drawn by the load is equal to the average value of the inductor current

The two MOS switches are turned on and off at an appropriate frequency and duty cycle to maintain the output voltage required. Defining the following operating parameters,

1. f = switching frequency
2. T = switching time period
3. T_{ON} = on-time for upper FET S1
4. T_{OFF} = off-time for upper FET S1 = on-time for lower FET S2
5. D = Duty Cycle = time that S1 is on relative to total switching time period

The basic timing relationships are:

1. $T = 1/f$
2. $T_{ON} + T_{OFF} = T$
3. $T_{ON} = D \bullet T$
4. $T_{OFF} = (1\text{-}D) \bullet T$
5. $0 \leq D \leq 1$

A typical inductor (L) current waveform versus time is shown in Fig. 2.

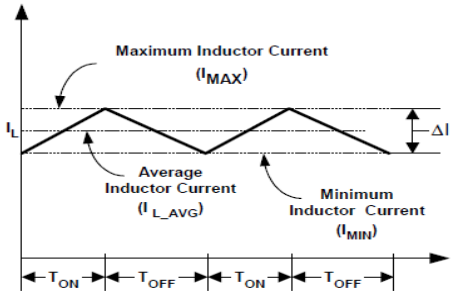


Figure 2. Inductor current waveform for two complete switching periods.

When the switch S1 is on, the input voltage is applied to the left side of the inductor and the current increases from an initial value of I_{MIN} in to I_{MAX} as shown during the T_{ON} portions of the waveform in Fig. 2. The relationship for voltage and current in an inductor is, as usual,

$$V_L = L \bullet \left(\frac{\Delta I}{\Delta T} \right) \quad (1)$$

Note that when S1 is ON, $V_L = (V_{IN} - V_{OUT})$ and $\Delta T = T_{ON} = D \bullet T$. We can now express the inductor ripple current as:

$$\Delta I = I_{MAX} - I_{MIN} \quad (2)$$

$$\Delta I = (V_{IN} - V_{OUT}) \bullet \frac{D \bullet T}{L} \quad (3)$$

During the time when S1 is turned OFF, the other switch S2 is turned ON. The inductor current ramps down during this portion of the cycle. When S2 is turned ON, the left side of the inductor is placed at ground potential (0 V). Maintaining the same sign convention, the differential voltage across the inductor (assuming an ideal switch S2) is:

$$V_L = (0 - V_{OUT}) = -V_{OUT} \quad (4)$$

The time period for this portion of the cycle is

$$T_{OFF} = (1 - D) \bullet T \quad (5)$$

and the corresponding change in current is

$$I_{MIN} - I_{MAX} = \Delta I \quad (6)$$

So, from the same relationship for inductor voltage and current, we obtain:

$$-V_{OUT} = L \bullet \frac{(-\Delta I)}{(1 - D)} \bullet T \quad (7)$$

$$V_{OUT} \bullet (1 - D) \bullet \frac{T}{L} = \Delta I \quad (8)$$

Since we now have two expressions for the ripple current ΔI which are equivalent, we can now relate the input to the output as a function of duty cycle, D:

$$(V_{IN} - V_{OUT}) \bullet \frac{D \bullet T}{L} = V_{OUT} \bullet (1 - D) \bullet \frac{T}{L} \qquad (9)$$

$$(D \bullet V_{IN}) - (D \bullet V_{OUT}) = V_{OUT} - (D \bullet V_{OUT}) \qquad (10)$$

$$D = \frac{V_{OUT}}{V_{IN}} \qquad (11)$$

At steady state operation, the average inductor current is at the midpoint of the maximum and minimum points shown in Fig. 2. This is also equivalent to the average load current as discussed previously. Thus,

$$I_{OUT} = I_{L\_AVG} = \frac{(I_{MAX} + I_{MIN})}{2} \qquad (12)$$

The current capability limitation of a given semiconductor converter chip stems from its peak switch current rating. This can be found in the IC data sheet. In the case of the TPS6230x series of devices, the minimum spec for the PMOS current limit is 670 mA, and the minimum specification for the NMOS is 550 mA. To protect itself from overcurrent damage, the IC does not allow the internal switch currents to exceed this level. The load current capability for the converter system is constrained by several factors: the switch current limit, the choice of external component (L), and the operating conditions (frequency and duty cycle).

It can be seen from Fig. 2 that the peak inductor current I_{MAX} is equal to the average inductor current plus half of ΔI (where ΔI = ripple current as shown in Fig. 2). Since the peak currents in S1 and S2 reach the same value as I_{MAX}, the highest possible load current is delivered when I_{MAX} is equal to the internal switch current limit for the IC.

$$I_{MAX} = I_{L\_AVG} + \frac{\Delta I}{2} = I_{OUT(\max)} + \frac{\Delta I}{2} = I_{SW\_LIMIT} \qquad (13)$$

$$I_{OUT(\max)} = I_{SW\_LIMIT} - \left(\frac{\Delta I}{2}\right) \qquad (14)$$

2.1 Buck Converter Summary

The value of I_{MAX}, the peak inductor current, cannot be allowed to exceed the peak switch current rating. Minimizing the ripple current will allow the output current to approach the peak switch current. Since the system designer cannot necessarily constrain the I/O voltage operating points, the only practical means of reducing the ripple current is to either increase the L value or decrease the on-time (T_{ON} = D●T) by increasing the switching frequency. The following general conclusions can now be made for the buck converter circuit:

1. At a given operating frequency, a large inductor has a lower ripple current, allowing the maximum output current to be higher.
2. For a given inductor value, choosing a higher operating frequency reduces the on-time, also allowing output current to approach the peak switch current limit.
3. The relative values of input and output voltage will also affect the relationship between the (internal) switch and (external) load currents. For a fixed output voltage, the ripple current increases with increasing input voltage.

By using the equations above and setting I_{MAX} (peak inductor current) equal to the IC's internal switch current limit, the maximum load current capability under different operating conditions and component

values can be calculated. Typical results are shown in Fig. 3 and Fig. 4.

It should be noted that for integrated converters with internal feedback loop compensation networks, the choice of external inductor must remain within a defined range as required for overall system stability. The internal compensation network is tuned to work with a specific range of L-C time constant for optimal stability. See reference [3] for further discussion of this aspect of converter design. In general, for a voltage-mode control architecture, if the inductor (L) is increased or decreased, the output capacitor (C) can be adjusted to maintain the same L-C product which affects the dominant pole of the control loop.

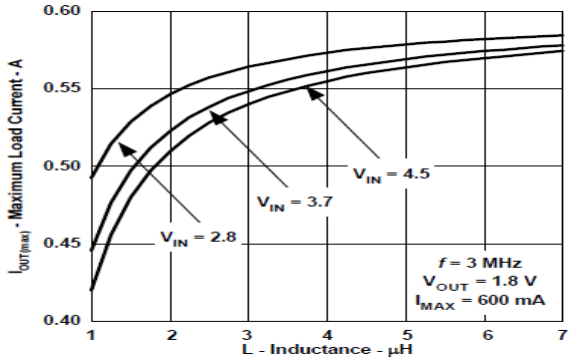


Figure 3. Ideal buck converter output current capability vs. inductance

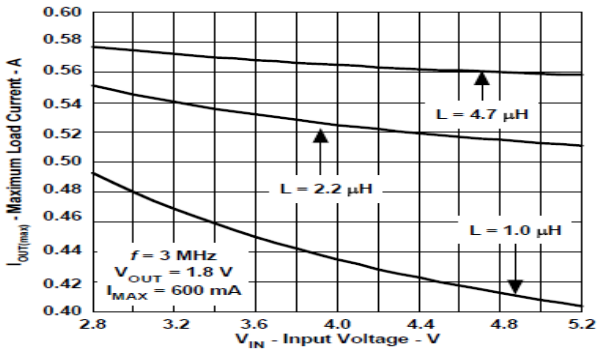


Figure 4. Ideal buck converter output current capability vs. input voltage.

In a practical design, the efficiency of the converter should also be considered in determining peak current capability. The derivations above for the ideal converter assume 100% efficiency; today's portable buck converters can often exceed 90% in practice so the results are not substantially different. The peak current rating for the ideal converter can be multiplied by the expected converter efficiency to obtain a closer approximation for a real design.

2.2. Buck Converter Test Results

The actual circuit implementation for a portable power converter closely resembles the idealized circuit at the schematic level. Fig. 5 shows the schematic of a 1.8-V, 500-mA output design using the TPS62303. Fig. 6 shows the actual circuit built on a PC board using two ceramic capacitors and a 1-µH chip inductor.

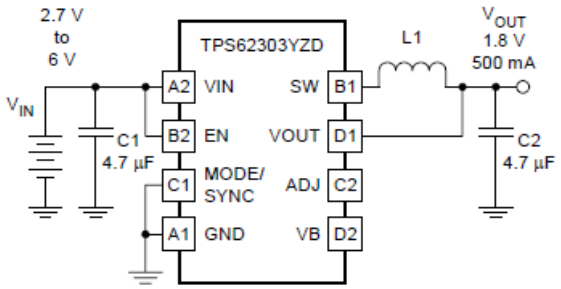


Figure 5. TPS6230x buck converter schematic.

Fig. 7 and Fig. 8 show oscilloscope traces of the inductor current for the TPS62300 device at moderately high load level (340 mA average output current, V_{IN} = 3.2 V, V_{OUT} = 1.8 V). Test results were measured using Tektronix TDS754 digital oscilloscope and TCP202 AC/DC current probes. It can be seen that the inductor ripple current in Fig. 7 is higher with the 1-µH inductor than in Fig. 8, with the 3.3-µH inductor. The peak inductor current cannot exceed the peak internal switch current, and a larger inductance value results in lower ripple current. Since the peak current is equal to the average load current plus half the ripple current, the use of a larger inductance value allows the output current to be slightly higher before the internal IC switch current limit is reached.

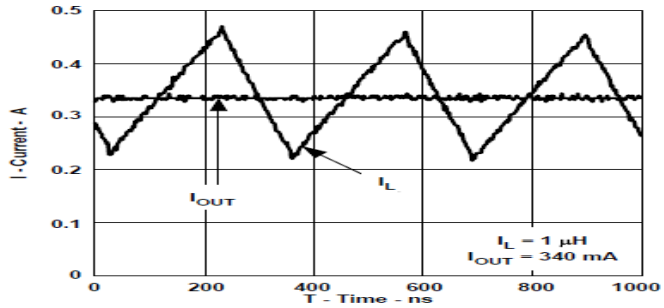


Figure 7. TPS62300 inductor current.

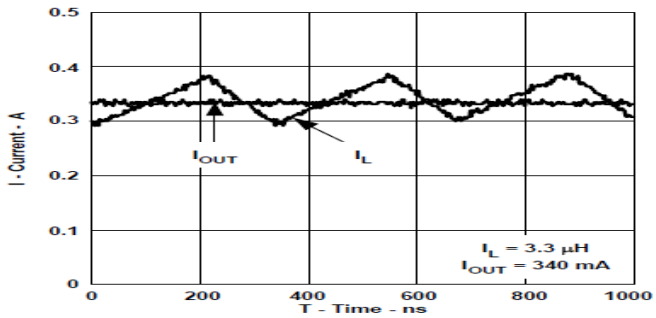


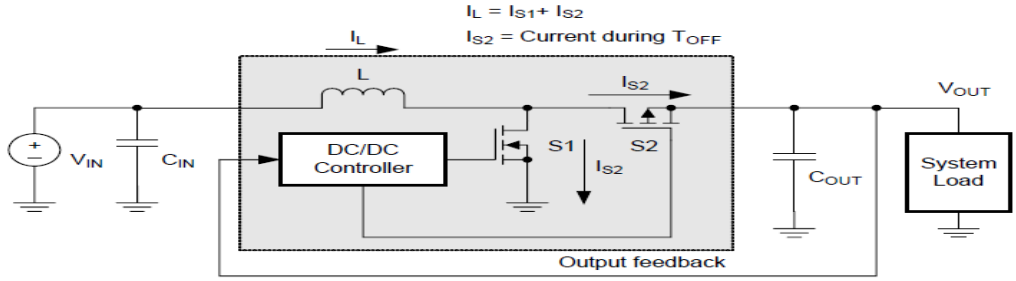
Figure 8. TPS62300 inductor current.

3. Boost Converter

The simplified synchronous boost converter topology is shown in Fig. 9. The inductor and switching

elements are rearranged from the buck topology in a manner that allows an output voltage to be generated that is higher than the input voltage. The two MOSFETs are operated in opposition as before, with only one of the two (S1 or S2) turned on at any given time. As discussed earlier, a traditional (non-synchronous) boost converter uses a diode in place of the output rectifier switch (S2); however in the ideal analysis both can be treated the same way since switch or rectifier loss is assumed to be zero.

In the earlier case of the buck converter, the L-C combination can be thought of simply as an output filter. The average output voltage is just a fractional portion of the input voltage, based on switch duty cycle, and the L-C smooths the pulse train at the switching node into a DC voltage. For the boost case, however, energy is not transferred directly from the input to the output when S1 is turned on. In the boost circuit, energy must first be stored in the inductor during the current ramp-up period when S1 is on, and then transferred to the output when S1 is OFF (and S2 is ON)



When S1 is turned ON, the inductor current steadily increases. Since S1 effectively shorts the right side of the inductor to ground, the voltage across the inductor is equal to the input voltage, and the current will increase at a constant rate:

$$\left(\frac{di}{dt}\right) = \left(\frac{V_{IN}}{L}\right) \qquad (15)$$

Note that in the boost topology, S1 can only be left on for a finite period of time; in other words the duty cycle cannot equal 100%. Otherwise, the inductor would eventually become saturated and the input voltage would effectively be shorted to ground.

When S1 is turned OFF, the current in the inductor begins to decrease. Since S2 is turned ON at this point, the inductor current now flows into the output capacitor and load. The inductor current is now decreasing, so (di/dt) becomes negative. Because of this, the polarity of the voltage across L reverses; the voltage at the right side of the inductor is now higher than the input voltage relative to ground. Since S2 is on only when the inductor is transferring energy into the output, the output voltage does not discharge back to a lower potential. This is how a boost converter generates an output higher than the input.

It is important to understand that the duty cycle (D) cannot practically reach the limit of 100% as can be done with the buck converter. In addition, the differences between continuous and discontinuous mode operation of the boost converter are significant. Since the topic of this section is to understand converter operation at high load currents, only continuous mode operation is discussed. See reference (2) for a derivation of discontinuous mode equations and a more complete discussion of the boost converter in general.

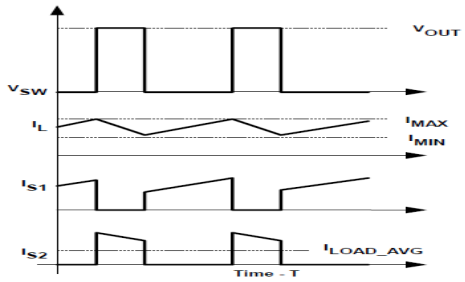


Figure 10. Boost topology.

Fig. 10 shows the switching node voltage and relevant branch currents in the boost topology. This particular example illustrates a steady-state condition corresponding to a 1:3 boost ratio and continuous inductor current. VSW is the voltage at the switch node to ground (the drain-source voltage of S1). The inductor current at any given time is the sum of the S1 and S2 current waveforms. The S2 current flows into the output capacitor and load. In steady-state operation, the output voltage is in regulation (DC) so the net current into the capacitor must be zero; thus the average of the S2 current is the average load current.

To determine the relationships between current and operating parameters for the boost circuit in the same manner as the buck circuit, the same symbols are used:

$$T = \left(\frac{1}{f}\right) \quad (16)$$

$$D = S1 \text{ duty cycle} \quad (17)$$

$$T_{ON} = D \bullet T \quad (18)$$

$$T_{OFF} = (1 - D) \bullet T \quad (19)$$

As before, determine the ripple current ΔI as a function of input voltage, output voltage, duty cycle, switching frequency, and inductance value. First, consider the inductor current-voltage relationship when S1 is turned ON (S2 is OFF). The inductor current increases from I_{MIN} up to I_{MAX} during the switch on-time of TON. The voltage across the inductor during this time is the input voltage V_{IN}. Using the following equations:

$$V_L = L \bullet \left(\frac{di}{dt}\right) \quad (20)$$

$$V_{IN} = L \bullet \left(\frac{(I_{MAX} - I_{MIN})}{T_{ON}}\right) = L \bullet \frac{\Delta I}{(D \bullet T)} \quad (21)$$

$$\Delta I = V_{IN} \bullet \left(\frac{D \bullet T}{L}\right) \quad (22)$$

During the time when S1 is OFF and S2 is ON, the inductor current decreases from its initial value of I_{MAX} to a final value of I_{MIN}. Using the same sign convention, the inductor differential voltage is (V_{IN} – V_{OUT}) since S1 is open and S2 is shorted. The duration of this downward ramp is T_{OFF}, so the equations

$$(V_{IN} - V_{OUT}) = L \bullet \left(\frac{(I_{MAX} - I_{MIN})}{T_{OFF}}\right) \quad (23)$$

$$(V_{IN} - V_{OUT}) = \Delta I \bullet \left(\frac{L}{(1-D) \bullet T} \right) \quad (24)$$

$$\Delta I = (V_{IN} - V_{OUT}) \bullet \left(\frac{(1-D) \bullet T}{L} \right) \quad (25)$$

Since there are two expressions for ΔI which must be equivalent in steady-state,

$$\left(\frac{V_{IN} \bullet D \bullet T}{L} \right) = (V_{OUT} - V_{IN}) \bullet \left(\frac{(1-D) \bullet T}{L} \right) \quad (26)$$

$$(D \bullet V_{IN}) = V_{OUT} - (D \bullet V_{OUT}) - V_{IN} + (D \bullet V_{IN}) \quad (27)$$

$$V_{IN} = (1-D) \bullet V_{OUT} \quad (28)$$

This shows that the boost ratio from input to output is

$$\left(\frac{V_{OUT}}{V_{IN}} \right) = \frac{1}{(1-D)} \quad (29)$$

Thus, a duty cycle of 90% yields an output voltage that is 10 times the input voltage. This is an approximate practical limit for single-inductor boost converters in continuous mode.

Since the peak instantaneous inductor current must be kept under the IC switch current limit, determine the average inductor current as a function of load current, and then add half the ripple current to determine the peak instantaneous inductor current. First, note that the average inductor current is the mid-point of the I_{MAX} and I_{MIN} values.

$$I_{L\_AVG} = \left[\frac{(I_{MAX} + I_{MIN})}{2} \right] \quad (30)$$

When S2 is ON (during the T_{OFF} period), its current is the same as the inductor current. When S2 is OFF (during the T_{ON} period, as the inductor current ramps up), its average current is zero. So, determine the average current in S2 during one entire switching cycle as

$$I_{S2\_AVG} = \left(\frac{T_{OFF}}{T} \right) \bullet \left(\frac{I_{MAX} + I_{MIN}}{2} \right) = (1-D) \bullet (I_{L\_AVG}) \quad (31)$$

Since at steady state (fixed input, regulated DC output, constant current load), the output current is equal to the average S2 current, we can the average inductor current is related to the load current as show in Equation (32).

$$I_{OUT} = (1-D) \bullet I_{L\_AVG} \quad (32)$$

Now there exists enough information to determine the maximum load capability of the boost converter. For a given load current I_{OUT}, and a known I/O voltage point,, determine the average inductor current required. For example, if the input is 3 V and output is 9 V, the duty cycle will be 0.67. So, to generate 9 V at 100 mA load current from a 3-V input, an average inductor current of (100/0.33) = 300 mA is required. This is the average amount of current required from the 3-V input source. Equations (33) and (34) can be used to determine the instantaneous peak current in the inductor for a given load current, inductor value and operating frequency.

$$I_{MAX} = I_{L\_AVG} + \left(\frac{\Delta I}{2} \right) \quad (33)$$

and

$$\Delta I = \left(\frac{V_{IN} \bullet D \bullet T}{L} \right) \qquad (34)$$

If the internal peak switch current limit in the device is known, set I_{MAX} equal to this value to determine the maximum load capability of the boost converter for a given operating condition.

$$I_{OUT(\max)} = (1 - D) \bullet \left(I_{SW\_LIMIT} - \frac{\Delta I}{2} \right) \qquad (35)$$

Fig. 11 and Fig. 12 show the variation in output current capability of a boost converter for different operating conditions.

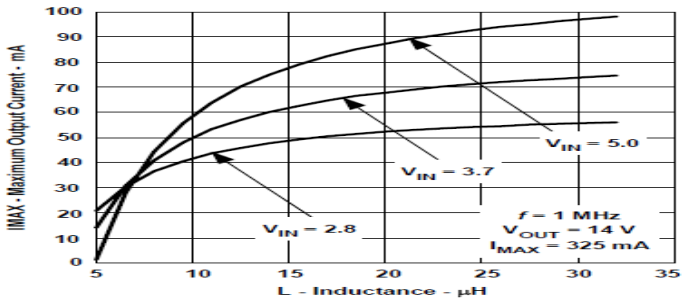


Figure 11. Ideal boost converter output current vs. inductance.

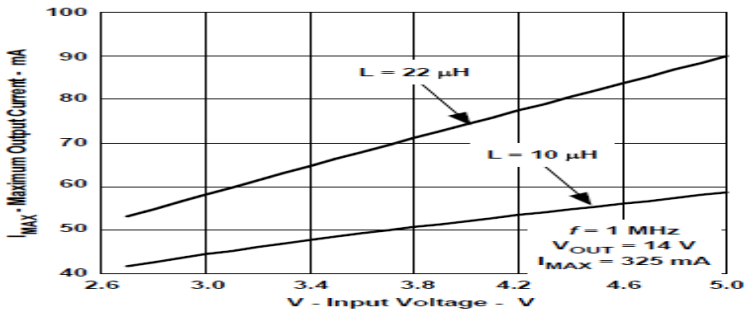


Figure 12. Ideal boost converter output current vs. input voltage

3.1 Boost Converter Summary

The boost converter shows the same tendency as the buck converter, in that larger inductance values reduce ripple current, and thereby allow higher load current.

It is important to note that the results shown for both cases assume zero losses (ideal converters). In an ideal converter, output power is equal to input power. For an actual converter, efficiency losses further reduce the output current available to the load.

As a first approximation, the ideal output current shown can be multiplied by the expected converter efficiency to obtain a practical estimate for output current capability. For example, 80% for a typical boost converter, or 90% for a typical buck converter.

3.2 Boost Converter Test Results:

Fig. 13 shows a typical application for the TPS61061 synchronous boost converter. The circuit shown generates a high voltage to drive a series string of LEDs for display backlighting. The boost converter can generate an output in excess of 16 V from a low voltage input. The exact output voltage in this case is dependent on the characteristics of the LEDs used and the brightness (current) level desired for the application. The feedback connection is configured to maintain a constant voltage across the sense resistor R_S, thereby controlling a constant current through the series string of LEDs.

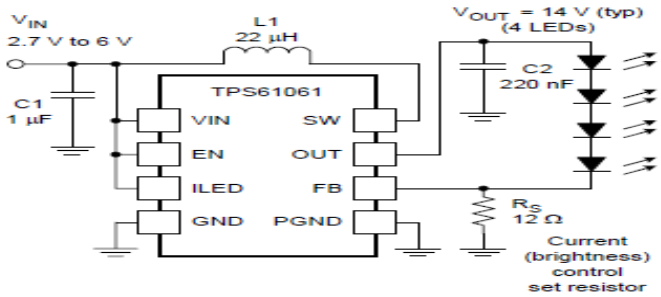


Figure 13. TPS61061 Synchronous boost converter.

As in the buck converter case, synchronous conversion will yield higher efficiency due to lower rectifier losses. At higher output voltage, this efficiency gain is not as significant. But, the synchronous approach has other advantages in portable applications. First, if integrated, the synchronous output FET reduces component count and size required for the total solution. Furthermore, internal gate control of the upper FET allows the output to be completely turned off when the converter is disabled. In a non-synchronous design, there is a DC leakage path from input to output through the diode even when the converter is turned off.

Fig. 14 and Fig. 15 illustrate the effect of different inductor values on the ripple current in a TPS61061 circuit. In these examples, an input of 3.0 V was used to generate an output of 13.9 V to drive four white LEDs at approximately 42 mA. Test results were measured using Tektronix TDS754 digital oscilloscope and TCP202 AC/DC current probes.

The ripple current in the case of the 10-µH inductor (Fig. 14) exceeds the worst case rating in the data sheet (325 mA) but not the typical rating (400 mA). Thus, a 10-µH inductor may be unacceptable if the desired LED current is in the range of 40 mA. With the 22-µH inductor (Fig. 15), we see that the peak ripple current stays just below the 325 mA worst-case switch current limit, so this value should produce a more reliable solution for a high brightness LED backlight application. These results correlate fairly well to the predicted values shown in Fig.11 and Fig. 12, which showed a best case output of about 45 mA for the lossless converter using a 10-µH inductor.

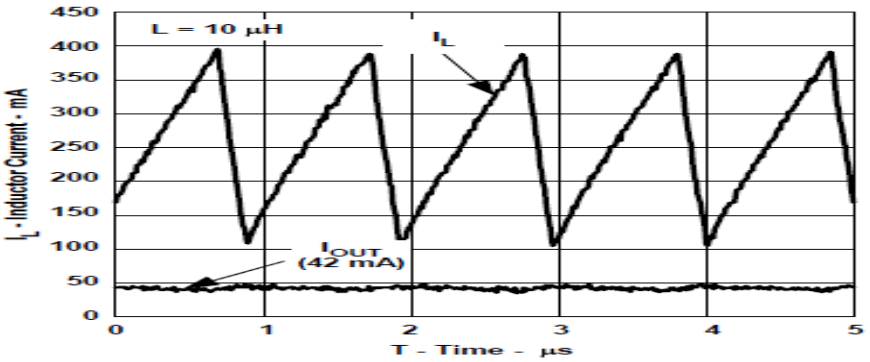


Figure 14. TPS61061 inductor current vs. time.

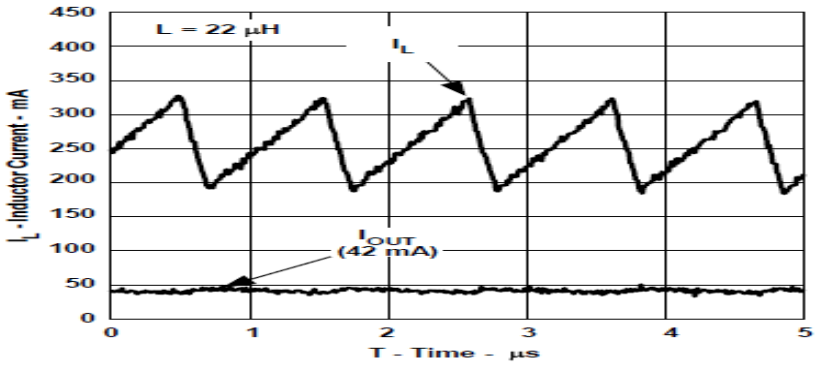


Figure 15. TPS61061 inductor current vs. time.

4. Conclusions

Because of the physical constraints of designing circuits for portable device applications, the system designer must often maximize power output for a given amount of board space. By understanding a few details of the operation of the power conversion subsystem, it may be possible to squeeze an extra few milliamperes from an integrated power converter without having to go to a larger or more expensive converter chip.

In the case of the buck converter, using a larger inductance value or a higher switching frequency helps achieve this goal. In the case of the boost converter, while the equations relating the input and output are quite different, the same general rules apply: larger inductance value or higher operating frequency allows the output current to increase for a given device's fixed switch current limit.

Conversely, if a given device solution has more than enough power capability for the application, it may be possible to slightly shrink the total solution size or cost by using a smaller inductance value. For two inductors having the same physical (package) size but different inductance values, the part with the lower

L-value usually has lower DC resistance (DCR) and higher saturation current rating (I_{SAT}). This generally results in higher efficiency. For two inductors having the same L-value but with different case sizes, the part that is physically smaller usually has higher DCR and lower I_{SAT}. If both L-value and physical size are decreased, the resulting (smaller) part may be acceptable since the higher DCR resulting from smaller package size (typically due to finer gauge wire) may be partially offset by the lower L-value (fewer winding turns).

As an example, if a 3.3-µH inductor is replaced with a physically smaller 1-µH inductor to shrink board space, the resulting circuit has higher ripple current and probably lower total output power capability. The 1-µH inductor yields a higher ripple current, and the smaller case size may increase DCR, lowering efficiency. If a 3.3-µH inductor is replaced by a 1-µH inductor having the same physical size, the output current capability may still be reduced only because of the higher resulting ripple current (see Fig. 3 and Fig. 11), but the efficiency may actually increase due to the lower DCR of the 1-µH part.

5. References:

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[5] Upal Sengupta, Getting the Most From Your Portable DC/DC Converter: How to Maximize Output Current for Buck And Boost Circuits. www.focus.ti.com