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Design of Low Voltage Improved performance Current Mirror

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Abstract

This paper proposes a low voltage current mirror circuit with low input impedance and high output impedance. These improvements are obtained by adding an amplifier which provides biasing voltage to the transistors. Its operation and results are compared with conventional and cascode current mirror circuits. The circuits are designed using Tanner EDA Tool in 90nm CMOS technology with 0.8V supply voltage. Simulation results shows that the minimum output voltage is reduced to 0.1 V, also input resistance is reduced to 0.179kΩ and consumes only 46μW power.

Keywords: Current mirror, Input resistance Output resistance, Input compliance voltage, Output compliance voltage.

1. Introduction

In analog circuit design, current mirror is used as a fundamental building block for a large number of integrated circuits like OTAs (operational trans-conductance amplifiers), Current Conveyors, CFOAs (current feedback operational amplifiers), filters etc [S. Chatterjee, Y. Tsividis, and P. Kinget (2005)]. Efficiency of a Current Mirror has had a direct impact on the overall performance of these integrated circuits. Relevant performance parameters of current mirrors in these applications include linearity in current transfer, power consumption, minimum supply voltage, input and output resistances [Paul R Gray, Paul J Hurst, Stephen H Lewis and Robert G. Meyer, A. S., Smith, K. C. (2005)]. One of the major drawbacks in conventional current mirror is their high input impedance and low output impedance. Many literatures have studied the problems of input impedance [S. C. Terry, M. M. Mojarradi, B. J. Blalock, and J. A. Richmond (2005), B. Aggarwal, and M. Gupta (2009), X.-G. Zhang and E. I. El-Masry (2004)]. Further a voltage amplifier is inserted between the drain and gate of input transistor to decrease the input impedance and also several possible implementations of the amplifier are studied. However these configurations suffer from poor stability problem. The better performance is achieved in case of using a differential amplifier [Nairn, D. G, Salama (1990)]. However drawback of differential amplifier is that it requires high supply voltage and more power consumption. The active input regulated cascode (AIRC) is further introduced with differential amplifiers in both input and output sides of current mirror and the circuit is claimed to have very low input and high output resistances [Serrano, T., Linares Barranco, B. (1994)]. Further, a current mirror is proposed which achieves low input impedance using flipped voltage follower (FVF) scheme. This scheme has some disadvantages of transient and bandwidth performance degradation, circuit complexity, and higher power consumption. Also it requires careful design of biasing network [Carvajal, R., Ramirez-Angulo, J., Lopez Martin, A., Torralba.A (2005)]. Current Mirrors based on alternative architectures such as bulk-driven, floating-gate, subthreshold etc are also presented. Bulk-driven based Current Mirror suffers from a lot of parasitics and reduced swing. In sub threshold current mirrors, the trans-conductance of the mirroring transistors is very low and hence their bandwidth is very poor also the current matching accuracy of these mirrors is also very low [Ramirez Angulo, J.Sawant, M.S. Lopez Martin, A., & Carvajal, R. G. Compact (2005), Naresh Lakkamraju, Ashish Kumar Mal (2011), Bradley A. Minch (2012)].

A current mirror is proposed which has low voltage, low input and high output impedances. The principle of operation of proposed current mirror is compared with simple current mirror. One of the major drawbacks of the conventional current mirrors is rather high input impedance, while especially in current mode signal processing the node impedances have to be very small. In fact this impedance has a substantial effect on overall dynamic range and frequency response of the circuit.

2. Conventional Current Mirror

A conventional Current Mirror structure (Figure 1) uses M1 in diode-connected configuration and the input

voltage V_{in} is required to pump input current I_{in} into the input port of the mirror. As evident, V_{in} depends solely on the biasing conditions of M1, which operates in saturation. Its trans-conductance g_{m1} decides the input impedance R_{in} of the Current Mirror.

For Conventional current mirror, input compliance voltage V_{in} is given by

$$V_{in} = V_t + \sqrt{2I_{in} / \beta i} \tag{1}$$

where,

V_t is the threshold voltage , $\beta_i = \mu C_{OX} \frac{W}{L}$, μ is the carrier mobility, C_{OX} is oxide capacitance. W and L refer to the width and length of the MOS transistors. The input current I_{in} is given as

$$I_{in} = \mu C_{ox} \frac{W_1}{L_1} (V_{GS} - V_t)^2 \tag{2}$$

From Figure 1, transistor M1 operating in saturation region which drives transistor M2 also in saturation and MOS transistor works as a constant current source. From equation (1) the lower limit of input voltage V_{in} of conventional current mirror is restricted to at least the value of the threshold voltage V_t. If the input current I_{in} is too low, this drives transistor M1 into sub-threshold region. The desired characteristics for current mirror circuit are to work under sub threshold operation, its input voltage $V_{in} = V_{ref}$ is sufficiently low (≤100 mV). To force M1 and M2 into sub-threshold region, one needs to increase the aspect ratios $\left(\frac{W}{L}\right)$ of these transistors which in turn lower the value of input voltage V_{in}. But circuits based on sub-threshold have poor frequency response and these circuits cannot be used in high frequency applications.

The output compliance voltage V_{out} required for Conventional Current Mirror is given by

$$V_{out} = V_{DS(sat)} \tag{3}$$

where,

$V_{DS(sat)}$ is drain to source saturated voltage.

The conventional current mirror suffers two major drawbacks; it requires an input compliance voltage which is always greater than a threshold voltage V_t and its output impedance is low. So this structure cannot provide requisite gains. One practice is to increase the output impedance of such a structure is to use cascode structure at the output port. The cascode Current Mirror of Figure 2 is the example of enhanced output impedance current mirror [P.E. Allen and D.R. Holberg, Holt, Rinehart and Winston(1987), R.L. Geiger, P.E. Allen, and N.R. Strader, D.A. Johns, K. Martin(1990), S.S. Rajput and S.S. Jamuar(2002)].

The input compliance voltage of cascode current mirror is given as

$$V_{in} = 2V_t + 2\sqrt{2I_{in} / \beta_i} \tag{4}$$

Input voltage of cascode current mirror is double of the input compliance voltage obtained with conventional current mirror of Figure 1. Hence, for low voltage applications, cascade current mirror shown in Figure 2 is not suitable and the analogue designers prefer single transistor at the input port while keeping the cascode structure at the output port as shown in Figure 3. Problem with this circuit is to provide suitable biasing voltage (V_b) for charging the gate of M3.

3. Proposed Current Mirror

In order to provide suitable biasing amplifiers of gain A_1 and A_2 are inserted in the proposed design which provides suitable biasing voltage to turn on transistor M3 and M4 respectively and provides high gain when working in saturation, as shown in Figure 4. Once transistor M4 is turned on, same output resistance as in cascode current mirror is observed. To obtain low input impedance, we incorporate transistor M3 in series with the input terminal of the basic circuit of the current mirror and use an amplifier of gain '$-A_1$' to control the gate voltage of transistor M3, Amplifier of gain A_2. Any increment in source voltage of transistor M3 (because of injected input current) causes its gate voltage to decrease '$-A_1$' times this works as stronger sink of input current which results in input impedance decrement by 'A_1'.

Figure 5 shows transistor level implementations of this idea which shows the amplifier can be implemented by only two transistors which act as a simple inverter for which input voltage is obtained as:

$$V_{in} = V_{sg3} + V_{ds5} \tag{5}$$

For the amplifier to have the significant gain required for perfect operation of the circuit, transistors M5 and M6 should operate in saturation region. If either of M5 or M6 is not in saturation condition, amplifier gain reduces and finally leading to increase in input impedance.

3.1 Input Resistance Analysis

Figure 6 shows the small signal equivalent circuit for the proposed circuit in which the direction of p-type current mirrors are drawn opposite to the direction of n-type. From Figure 7 we get,

$$V_{gs5} = V_{sg6} = V_{in} \tag{6}$$

$$V_{s4} = V_{s5} = 0 \tag{7}$$

$$V_{gs3} = -(g_{m5}V_{gs5} + g_{m6}V_{gs6})(r_{ds5} \| r_{ds6}) \tag{8}$$

$$V_{gs3} = (g_{m5} + g_{m6})(r_{ds5} \| r_{ds6})V_{in} \tag{9}$$

With reference to the basic proposed circuit of Figure 4, the voltage gain A_1 is defined as

$$A_1 = -\frac{V_{gs3}}{V_{in}} \tag{10}$$

Using equation (6) to (9), this simplifies to

$$A_1 = (g_{m5} + g_{m6})(r_{ds5} \| r_{ds1}) = (g_{m5} + g_{m6})/(g_{ds5} + g_{ds6}) \tag{11}$$

$$V_{in} = I_{in}\left[\frac{1}{g_{m1}} \| r_{ds1}\right] + (g_{m3}V_{gs3} + I_{in})r_{ds3} \tag{12}$$

$$\cong I_{in}\left[\frac{1}{g_{m1}}\right] + (g_{m3}V_{gs3} + I_{in})r_{ds3} \tag{13}$$

$$V_{gs3} = V_{g3} - V_{S3} = -(A_1 + 1)V_{in} \tag{14}$$

$$V_{in} = I_{in}\left[\frac{1}{g_{m1}}\right] - g_{m3}r_{ds3}(A_1 + 1)V_{in} + I_{in}r_{ds3} \tag{15}$$

$$V_{in}g_{m3}r_{ds3}(A_1 + 1) = I_{in}\left[\frac{1}{g_{m1}} + r_{ds3}\right] \tag{16}$$

The input impedance R_{in} then obtained as

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{\left[\frac{1}{g_{m1}} + r_{ds3}\right]}{1 + g_{m3}r_{ds3}(A_1 + 1)} \cong \frac{r_{ds3}}{1 + g_{m3}r_{ds3}(A_1 + 1)} \tag{17}$$

From analysis it is clearly observed that the input resistance of proposed current mirror circuit depends on the amplification gain A_1. Higher the amplification gain, the lower will be the input resistance and in order to achieve higher gain, it is necessary that both transistor M7 and M8 (PMOS and NMOS) should work in saturation region.

3.2 Output Resistance Analysis

The small signal circuit for calculating the output resistance of proposed current mirror is given in Figure 7. Applying KCL at the output node in Figure 7 we get-

$$I_{out} = g_{m4}V_{gs4} + r_{ds4}(V_o - V_{s4}) \tag{18}$$

$$I_{out} = g_{m4}(V_{g4} - V_{s4}) + r_{ds4}V_o - r_{ds4}V_{s4} \tag{19}$$

$$A_2 = V_{g4}/V_{s4} \tag{20}$$

$$V_{gs} = A_2V_{S4} \tag{21}$$

$$I_{out} = g_{m4}V_{gs4}(A_2 - 1) + r_{ds4}V_o - r_{ds4}V_{s4} \quad (22)$$

$$V_{s4} = I_{out}r_{ds2} \quad (23)$$

Putting all the values, we get

$$I_{out}(1 + g_{m4}r_{ds4}(A_2 - 1) + r_{ds2}r_{ds4}) = V_o r_{ds4} \quad (24)$$

The output impedance R_o is given as

$$R_o = V_o / I_{out} = (1 + g_{m4}r_{ds2}A_2 + r_{ds2}r_{ds4}) \quad (25)$$

$$R_o = g_{m4}r_{ds2}r_{ds4}A_2 \quad (26)$$

Output resistance of proposed mirror circuit is equivalent to cascode current mirror and also it depends on amplification gain A_2. Higher the amplification gain of amplifier, more will be its output resistance.

4. Simulation Results for existing current mirrors

Simulations are carried on Tanner EDA Tool on 90nm CMOS technology utilizing 1 V power supply. Input characteristic, output characteristic and frequency response of existing current mirror are simulated. The bias current is taken as 50 µA on which the ac input current is superimposed.

4.1 Input characteristic of Conventional and Cascode current mirror

Figure 8 shows the input characteristic of conventional current mirror circuit which shows a variation of input current from 0 to 1.5 mA over the input voltage varying from 0 to 1.0 volts. Because of single transistor at the input side in conventional current mirror, it shows minimum input compilance voltage of 0.4 V. For a companion, the input characteristic of cascode current mirror circuit is shown in figure 9. A notable change in input characteristic of cascode current mirror is obtained due to reduced resistance. The minimum input compilance voltage in this case is 0.6V.

4.2 Output characteristic of Conventional and Cascode current mirror circuit

In VLSI design, output resistance of current mirror should high so that proper matching between circuits will take place. Ideally it should be infinite but practically its value is limited. Figures 10 and 11 shows the output characteristics of conventional current mirror and cascode current mirror, respectively. Cascode current mirror shows better results because of cascoding (one transistor over another). The reduction in output current of Figure 11 as compared to Figure 10 is an indication that the output resistance of cascode current mirror is high.

4.3. Frequency response of Conventional and Cascode Current Mirror circuit

The bandwidth of operation of conventional current mirror is wider than that of cascode current mirror, as evident from the frequency response characteristic of circuits shown in Figure 12 for conventional and Figure 13 for cascode current mirrors. Formation of series capacitance increases the bandwidth in conventional current mirror while in cascode current mirror, there is parasitic capacitance in parallel which degrade its frequency response.

5. Simulation Results for proposed current mirror

5.1 Input characteristic of proposed Current Mirror circuit

It is desirable for low voltage operation that M1 and M2 operate either in sub-threshold or in saturation region. PMOS transistor is added in series with NMOS transistor which works as a current source. By applying proper biasing voltage, the turn on condition of PMOS transistor will ensure NMOS transistor to work in saturation region. Also when M7 and M8 enter into saturation region, this in turn, lowers the input resistance. The minimum input voltage of proposed current mirror is obtained as 0.3V. Figure 14 shows the input characteristic of proposed current mirror.

5.2 Output characteristic of Proposed Current Mirror circuit

The minimum output voltage of the proposed current mirror is reduced to 0.1V as observed from Figure 15. Also high swing at output is obtained. Reduction in $V_{\min(out)}$ is because of cascoding of transistors.

5.3 Frequency response of proposed Current Mirror circuit

The current through M4 should be small enough to keep M4 in sub-threshold region. Correspondingly W/L ratio should also be large. This will increase the device capacitance and bandwidth. Figure 16 shows a frequency response of proposed current mirror. From this figure a bandwidth of 98.45 MHz is obtained.

6. Conclusion

A novel structure to improve conventional current mirror's input impedance and output impedance is introduced. The principle of the input impedance reduction and increment of output impedance is discussed. A comparison between the features of the proposed current mirror and the basic and cascode current mirrors is presented both in analytic and simulation format. It is shown that input impedance is reduced and output impedance is increased significantly as compared to that of the simple current mirror. Simulations are carried on Tanner EDA Tool on 90nm CMOS technology are presented to demonstrate the performance validation of the proposed current mirror. As is shown the proposed current mirror achieves low input impedances and high output impedance without degrading other specifications.

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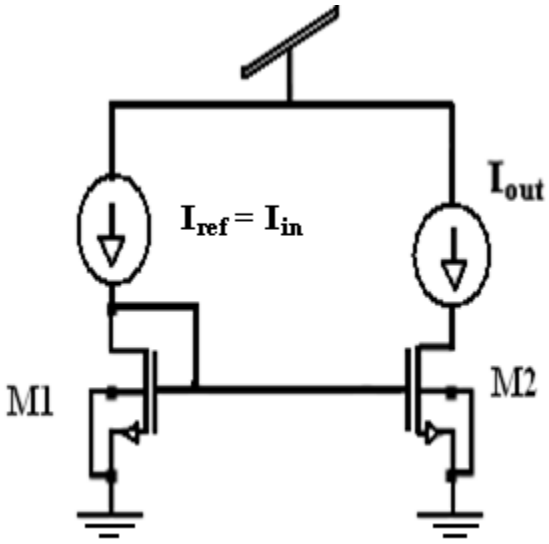

Figure 1. Conventional Current Mirror circuit

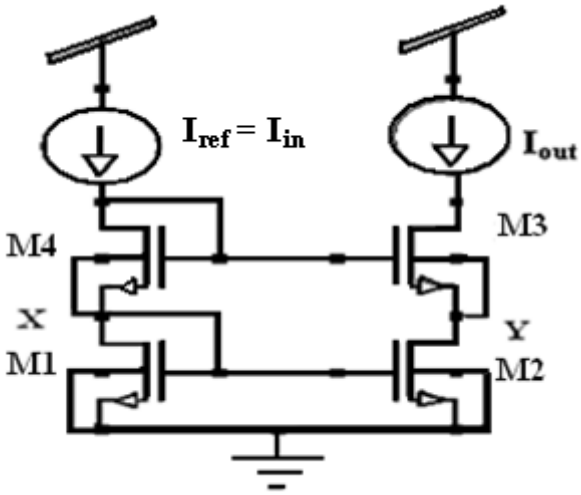

Figure 2. Cascode Current Mirror circuit

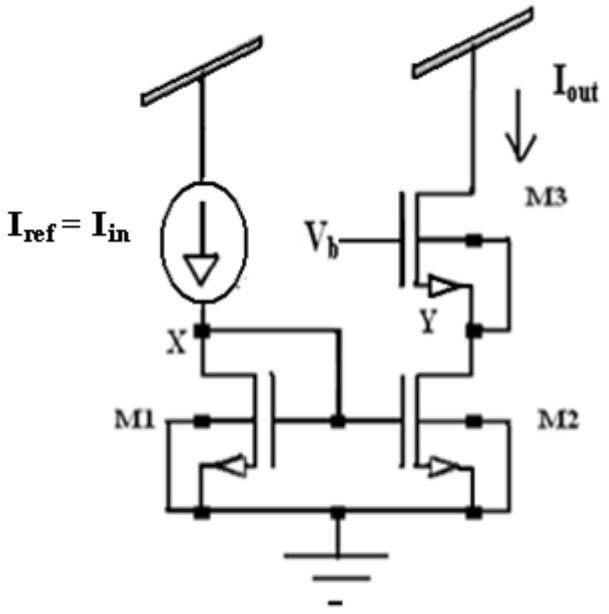

Figure 3. Current Mirror Circuit with single transistor at the input port

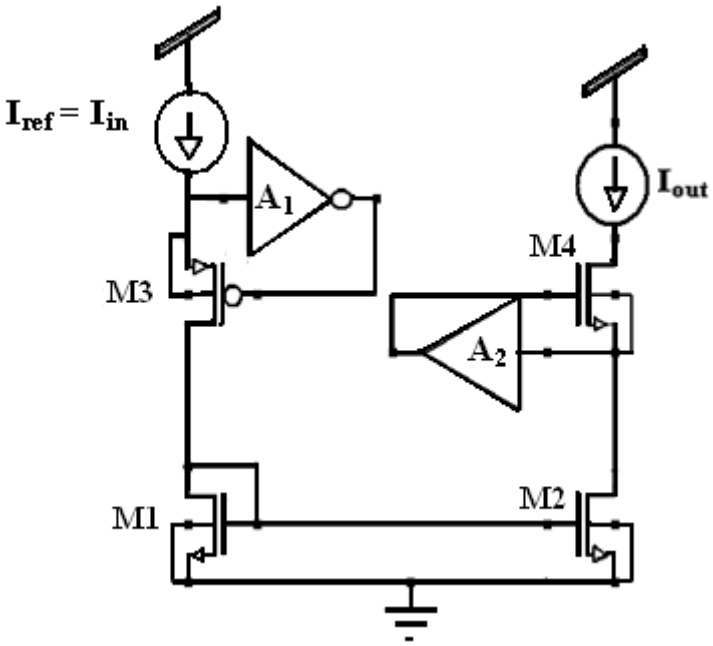

Figure 4. Proposed Current Mirror circuit with amplifiers for bias voltage

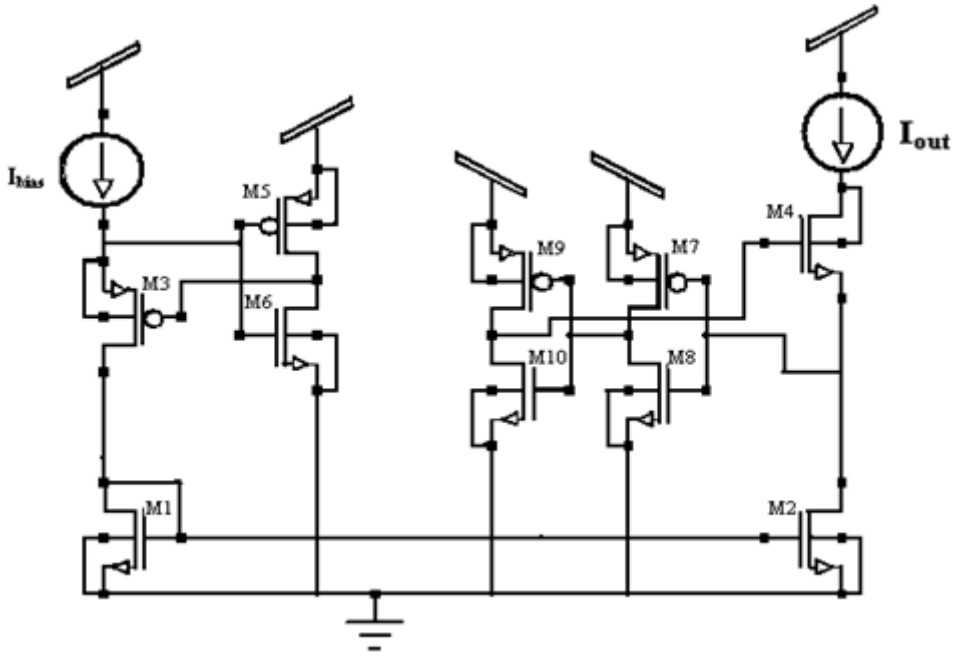

Figure 5. Transistor level implementation of Proposed Current Mirror circuit

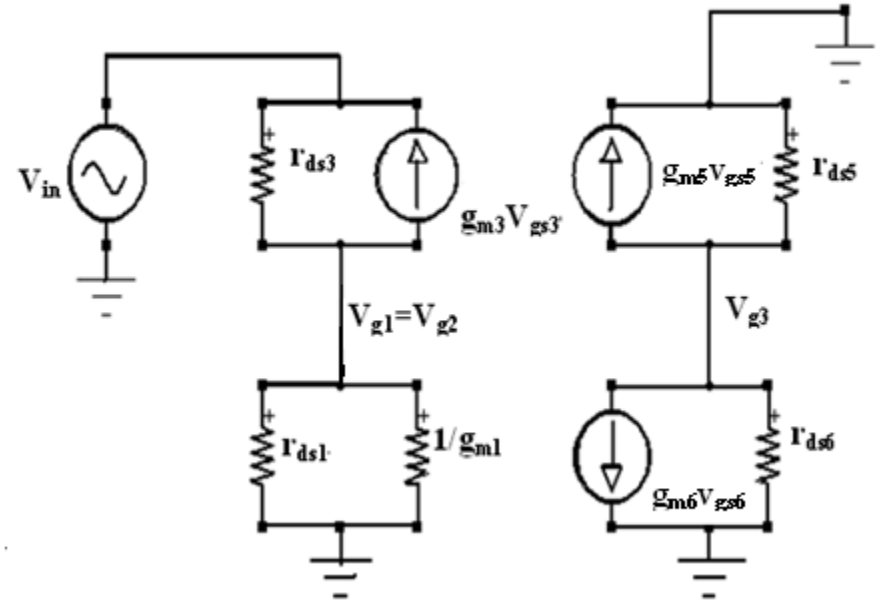

Figure 6. Small signal analysis of proposed circuit for calculating input resistance

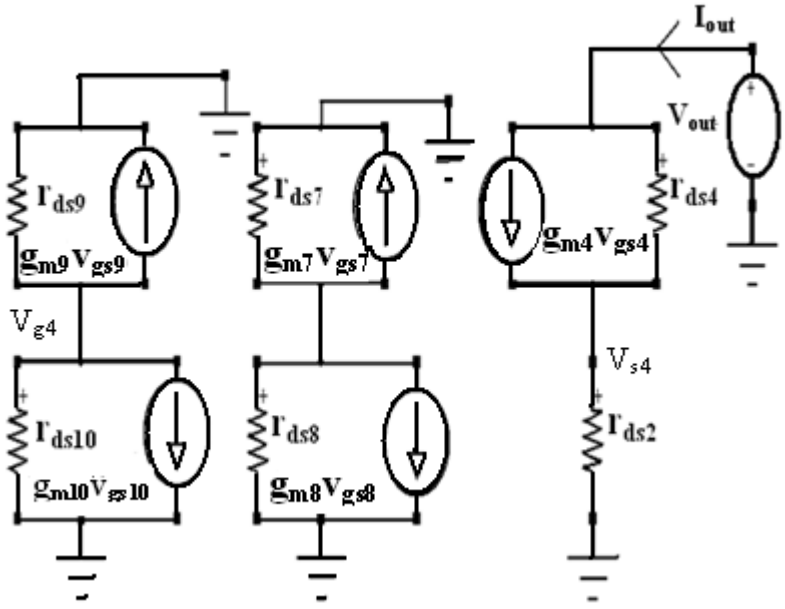

Figure 7. Small signal analysis of proposed circuit for calculating output resistance

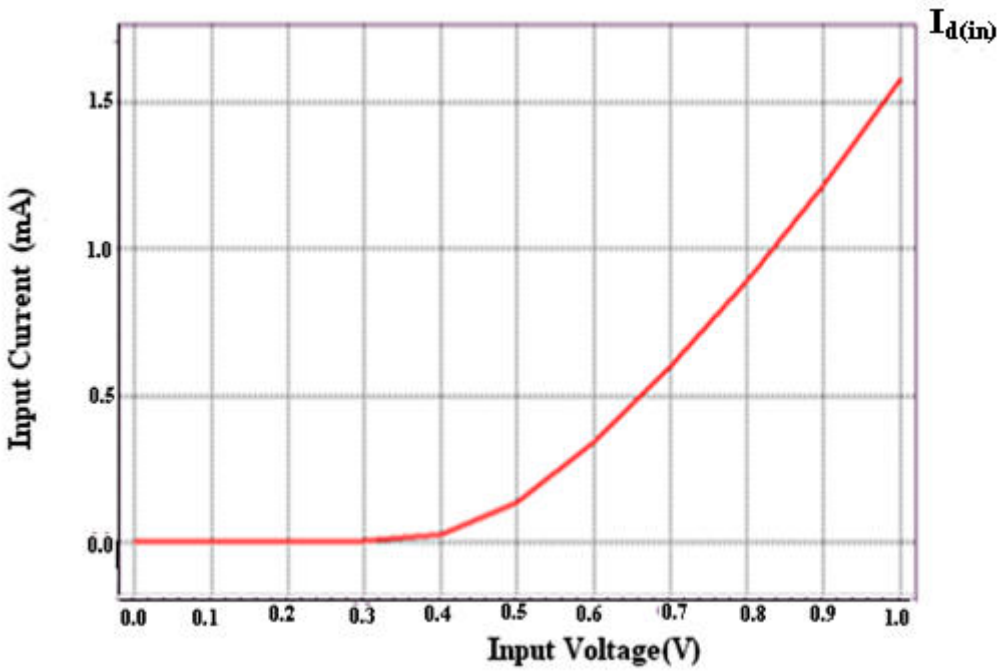

Figure 8. Input characteristic of Conventional Current Mirror circuit

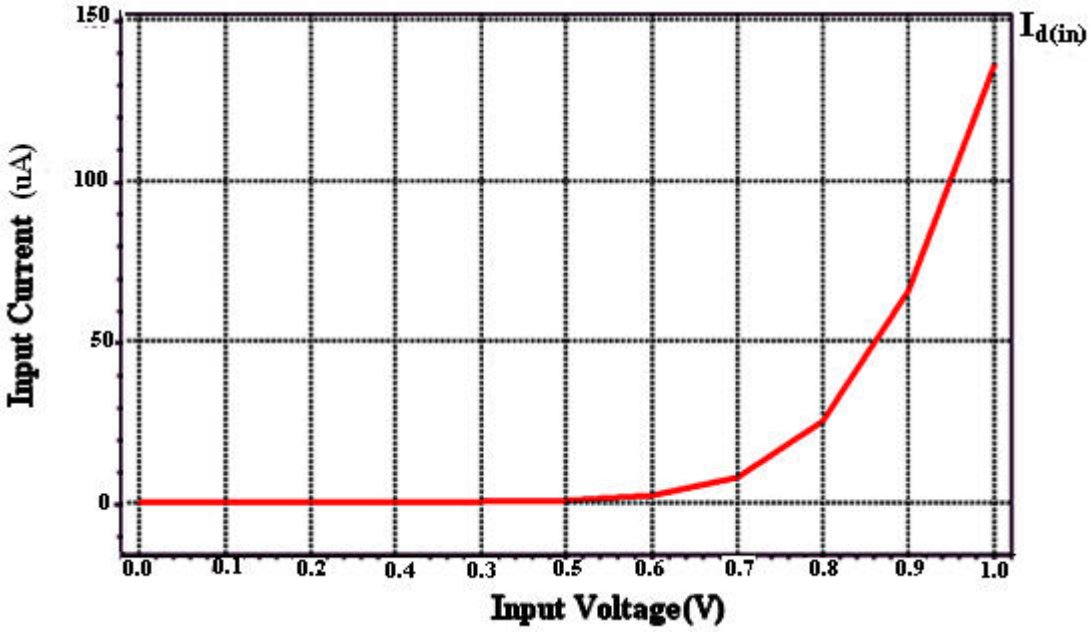

Figure 9. Input characteristic of Cascode Current Mirror circuit

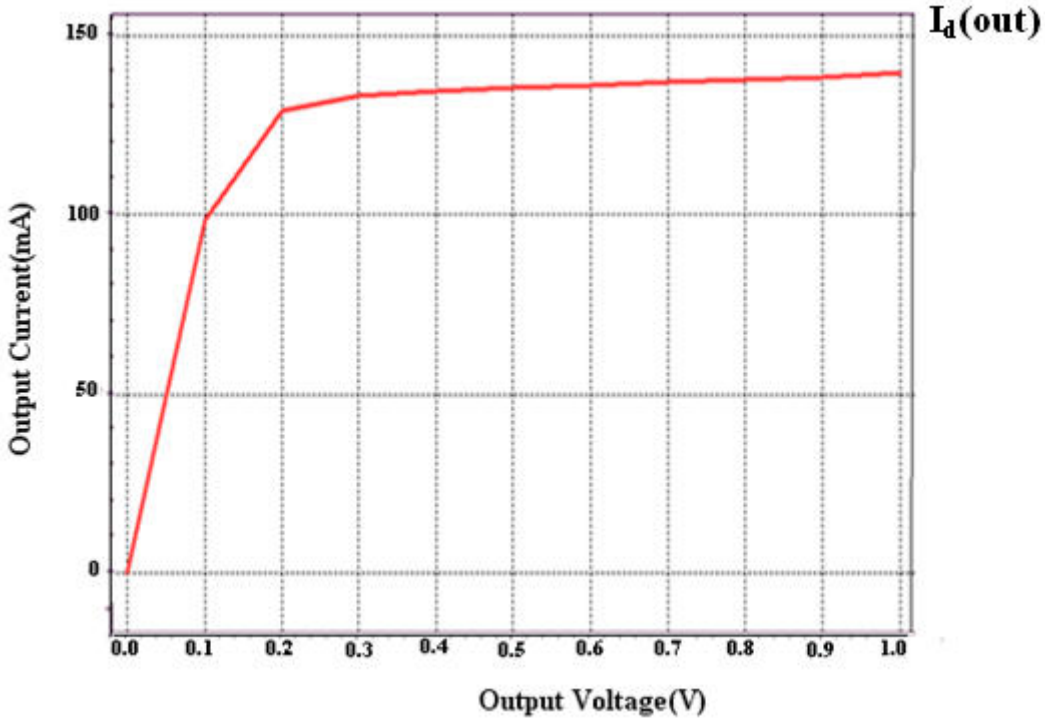

Figure 10. Output characteristic of Conventional Current Mirror circuit

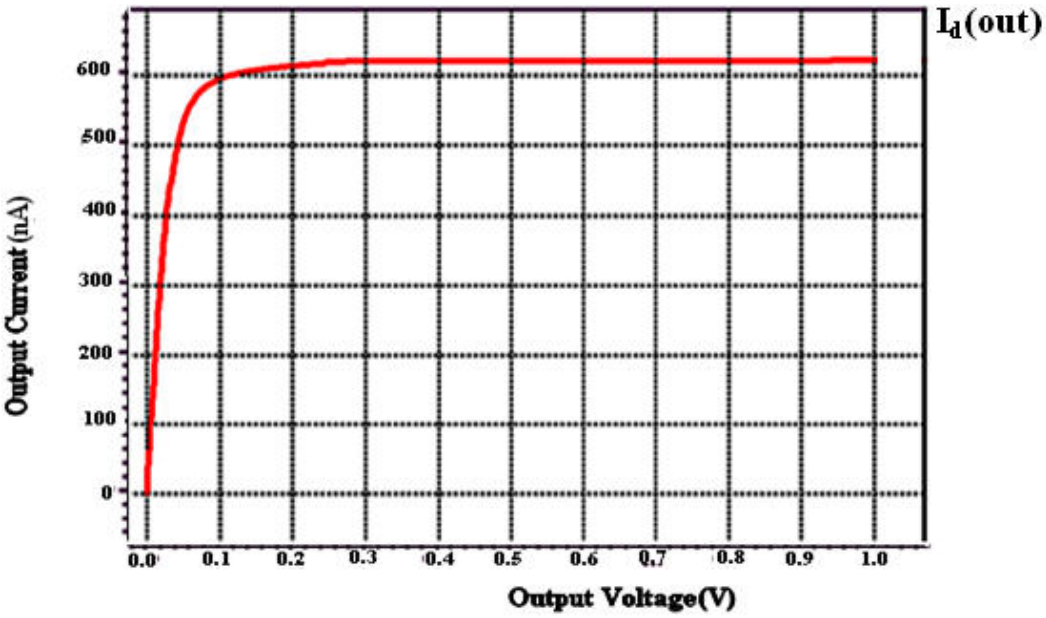

Figure 11. Output characteristic of Cascode Current Mirror circuit

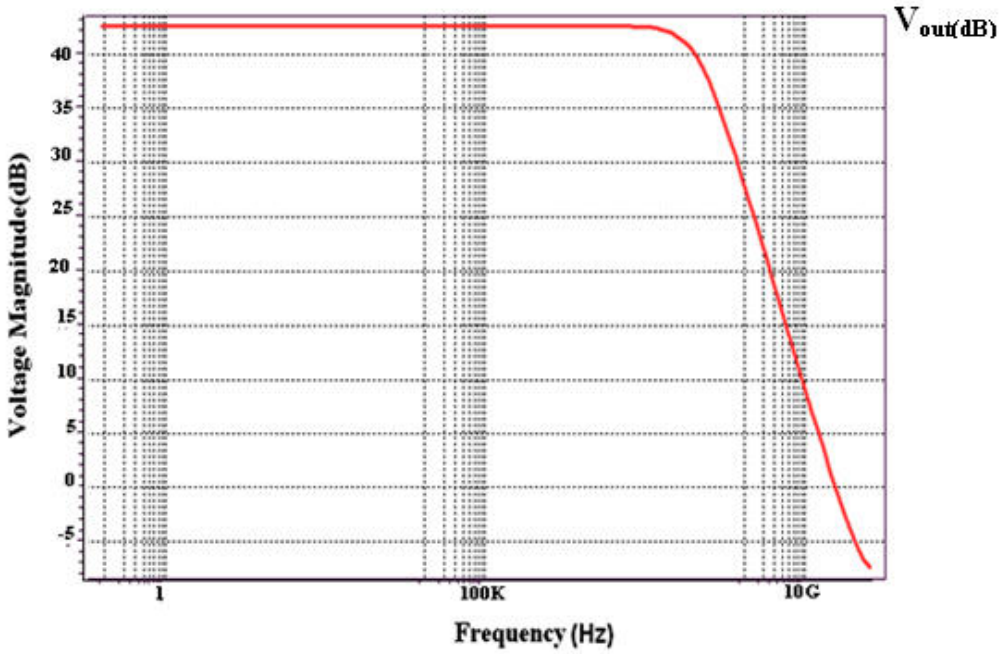

Figure 12. Frequency response of Conventional Current Mirror circuit

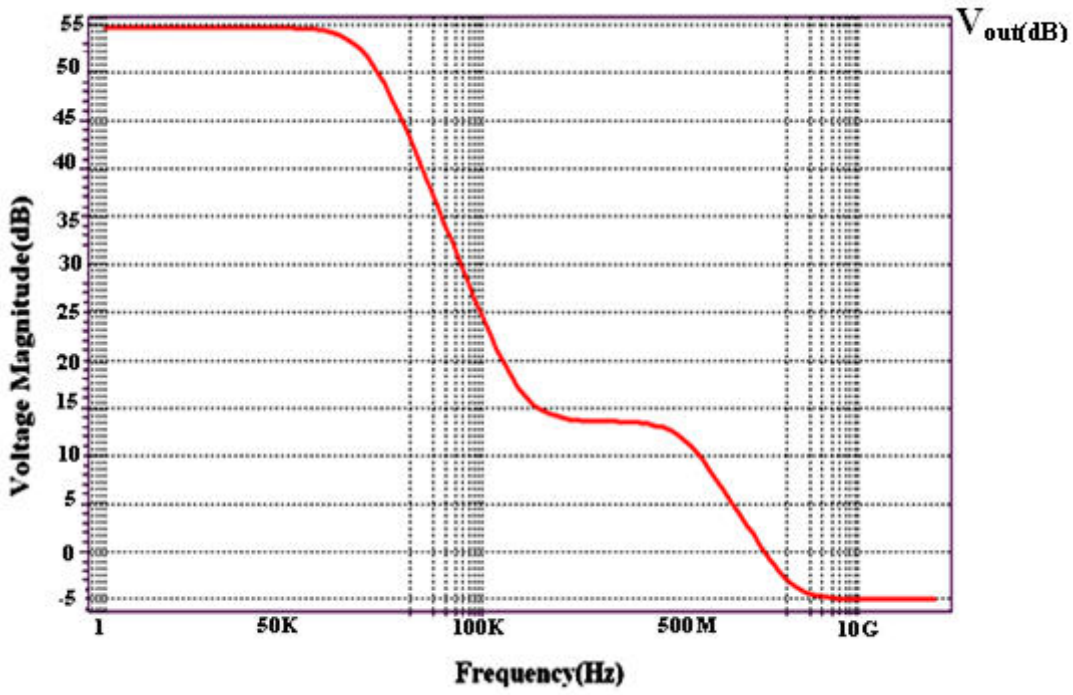

Figure 13. Frequency response of Cascode Current Mirror circuit

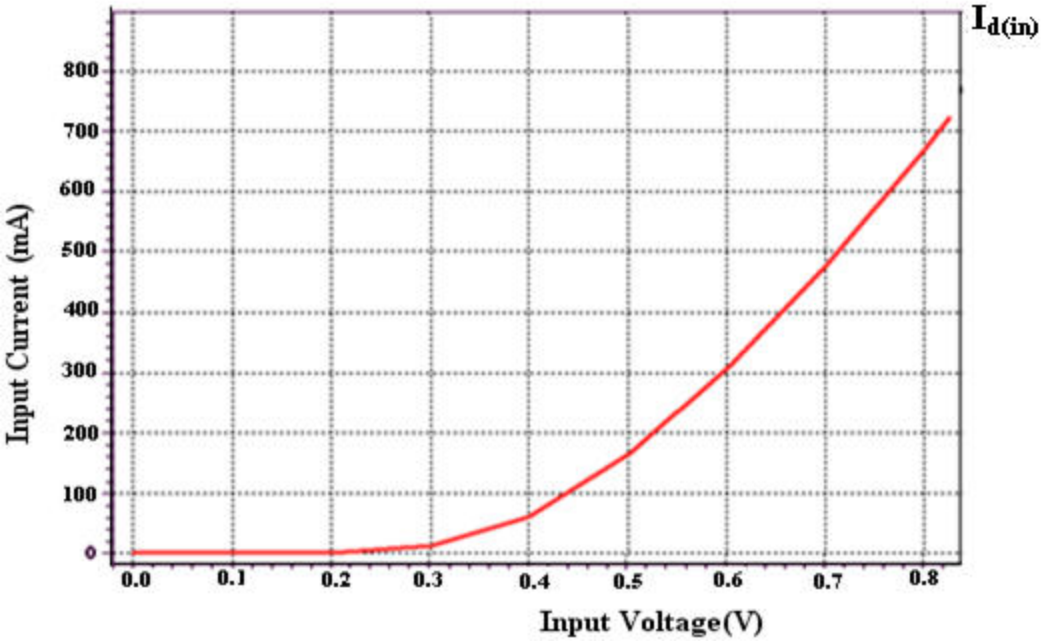

Figure 14. Input characteristic of proposed Current Mirror circuit

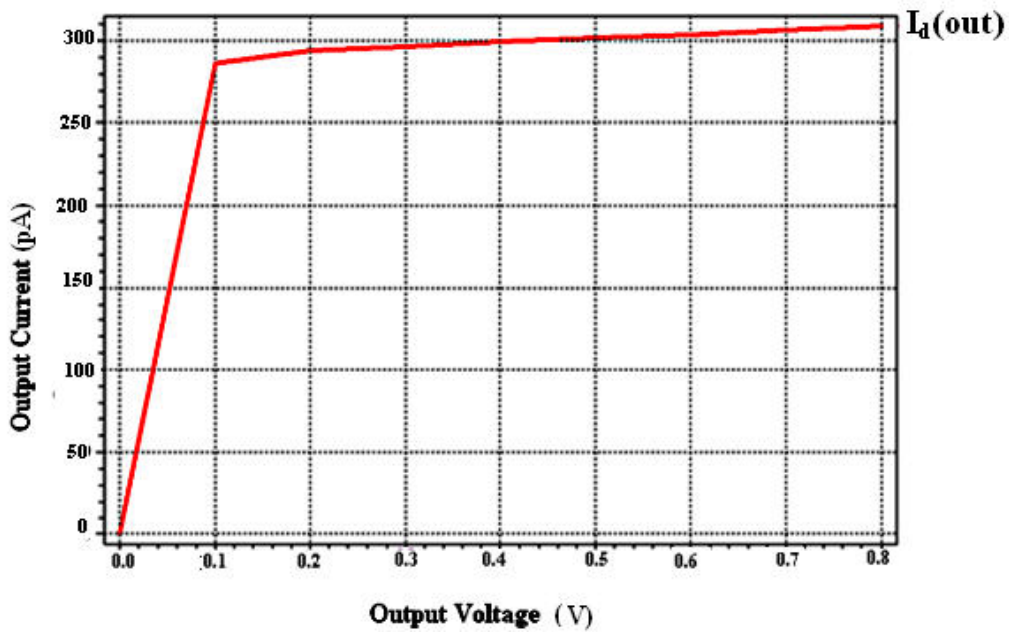

Figure 15. Output characteristic of Proposed Current Mirror circuit

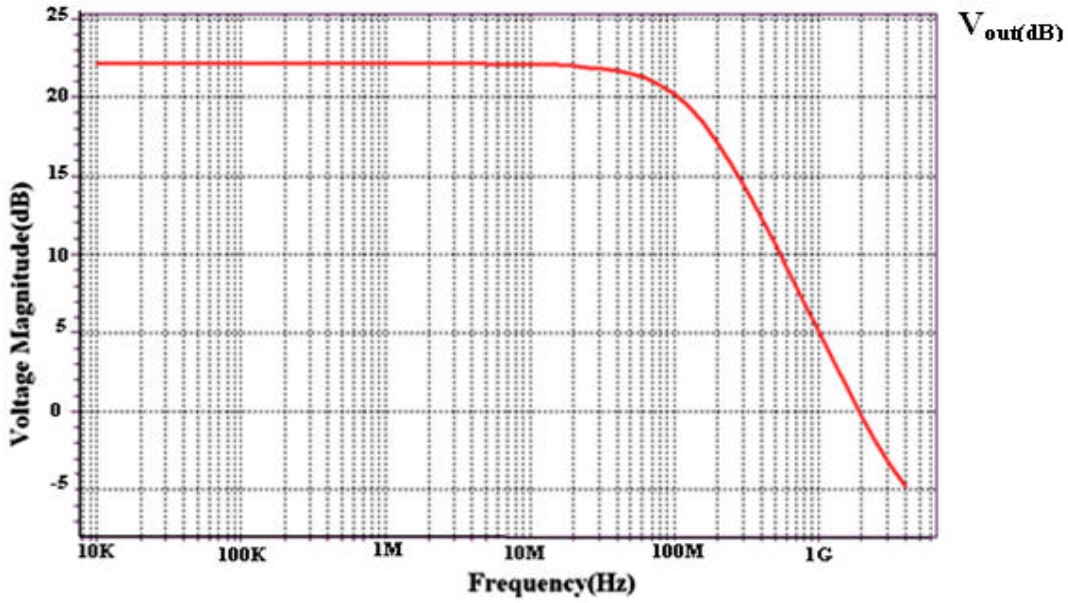

Figure 16. Frequency response of Proposed Current Mirror circuit

Table1. Comparison between Conventional, Cascode and proposed Current Mirrors at 90 nm technology

	Conventional Current Mirror	Cascode Current Mirror	Proposed Current Mirror
Supply Voltage	1.0V	1.0V	0.8V
Minimum Input Voltage	0.4	0.6	0.3
Minimum Output Voltage	0.2	0.1	0.1
Input Resistance	0.2020KΩ	59.460KΩ	0.1790KΩ
Output Resistance	125.16 KΩ	2.756MΩ	6.247MΩ
Bandwidth	876MHz	95.8 KHz	98.45MHz
Power Consumption	52.8 µW	74.186 µW	46 µW