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Single Edge Triggered Static D Flip-Flops: Performance Comparison

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Abstract
Due to fast growth of portable devices, power consumption and timing delays are the two important design parameters in high speed and low power VLSI design arena. In this paper we presents the comparison of single edge triggered static D flip-flop designs to show the benefit of power consumption ,delay and power delay product on the basis of area efficiency.
Keywords: Single edge triggered flip-flops, super-threshold region, parasitic capacitance, transmission gate

1. Introduction

High speed operations have become important in the modern designs of several electronics component. Flip-Flops are extremely important circuit elements in all synchronous VLSI circuits. It is estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 20%–45% of the total system power [1]. Moreover, flip-flops have a large impact on circuit speed. Therefore the improvement of such circuits such as a decrease in power consumption, without weakening other characteristics, is of the basic concern of the VLSI industry.

A conventional single edge-triggered (SET) flip-flop typically latches data either on the rising or the falling edge of the clock cycle and offers better performance in terms of both power consumption and speed as compared to double edge triggered flip-flop [2]. The flip-flops can also be categorized based on whether they are dynamic or static, in nature of their operation. In the case of dynamic flip-flops the charge stored at transistor node capacitances, leaks away in the transistor's 'OFF' state (clock stopped) and thus can produce faulty logic levels. On the other hand, the static flip-flops maintain their state even when the clock is stopped and power is maintained [3].

The paper is organized into three sections. Section I gives the introduction about the recent trends and necessities of designing the flip-flop circuit. Section II illustrates the different single edge triggered static D flip-flops. The comparative analysis of different single edge triggered static D flip-flops as reported in the literature included in Section III and finally Section IV concludes the paper.

2. Single edge triggered static D flip-flops

2.1 Conventional SET D flip-flop

The circuit shown in Figure 1 shows a single edge triggered (SET) D flip-flop with 18 transistors (including an inverter to produce complementary clock signals) [4]. A dashed vertical line has demarcated the Master and Slave sections. The master section of 18T D flip-flop consists of D latch, which is functional and transfer the data input D to intermediate node P on positive level of clock signal. There is a feedback loop L1 that maintains the logic level at the node P when the clock signal goes to logic level low. Similarly, the Slave section consists of a D-latch, which is functional on the negative level of the clock and transfers the logic level at intermediate node P to the output node Q. Again, there is a feedback loop L2 that maintains the logic level at node Q when clock signal goes to logic level high.

2.2 12-Transistor (12T) D flip-flop

12T SET D flip-flop design is illustrated in Figure 2.This design is formed by using three inverting gates, two pass transistors and a transmission gate (an including an inverter to produce complementary clock signals). This flip-flop also formed using master-slave flip-flop design .Master latch become active when the clock signal is high and slave latch become active when clock signal is low [5].

The master latch of 12T SET static D flip-flop become active when the clock signal is high and transfer the input din signal to inverting gate. When clock signal is low inverse of clock signal i.e., clkb signal is high, slave section become transparent and output of the master latch is entered into the slave latch of D flip-flop design. This signal is then passed through two inverters and outputs 'q' and 'qb' are obtained. When clock signal is active high and inverse of clock signal ,i.e. clkb is active low, the transmission gate, which is forming the feedback path, becomes transparent and output is fed back. Even if the clock is stopped (permanently grounded) the 12T flip-flop circuit is able to maintain the logic levels at q and qb, which proves the fact that the existing SET is static in nature.

In the layout design of the 12T flip-flop (Figure 3), number of poly contacts is three and number of

poly and metal overlap is two.

2.3 11-Transistor (11T) D flip-flop

11T SET static D flip-flop design is illustrated in Figure 4.This design is formed by using two inverting gate, two transmission gate, and one pass transistor (including an inverter to produce complementary clock signals) ,so total transistor used in this design is eleven.[6]. The transmission gate produces the full output swing.

In this design, transmission gates are using in master and slave section instead of using pass transistor. The master latch of 11T SET static D flip-flop become active when the clock signal is high and inverse of clock signal i.e. clkb is low ,transmission gate takes the data input din signal and transfer this signal to inverting gate. When clock signal is low and inverse of clock signal i.e. clkb is high, transmission gate of slave section become turn on and at the same time transmission gate of master latch turns off and output of the master latch is entered into the slave latch of D flip-flop design. This signal is then passed through an inverter and output q is obtained. When clock signal is active low, the pass transistor, which is forming the feedback path and output is fed back through transistor PMOS_6, therefore output is preserved. This operation of the circuit confirms the static behavior of the flip-flop.

In the layout design of the 11T flip-flop(Figure 5), number of poly contacts is three and one metal to poly overlap.

3. Comparative Analysis

The SET static D flip-flop designs have been simulated with SPICE Tool at 65nm process technology in super threshold region with same testing conditions.

The waveform of the SET D flip-flop design shows that it is a negative edge triggered flip-flop. The output changes at negative edge of the clock and remains constant during the positive edge of the clock.

3.1. Variation with Voltage

To operate in super threshold region, the supply voltage and the input voltages are kept always above the threshold voltage .When voltages are varied then accordingly power consumption changes, power consumption goes to increase as voltage increases because theoretically, power consumption is proportional to the square of the supply voltage. The power consumption of 11T flip-flop is approximately same as compared to 12T flip-flop but the delay (Figure 6)and power delay product (Figure 7) of 11 T flip-flop is remarkably low than 12T flip-flop.

3.2 Variation with Temperature

As the simulations have been carried out in super threshold region i.e. voltage applied is more than the threshold voltage of the MOSFETs, therefore power consumption of the device increases with temperature as the carrier collision rate increases and the power is consumed in the form of thermal energy. The delay (Figure 8) and power delay product (Figure 9) introduced by 11 T flip-flop is comparatively very less than 12T flip-flop.

It is also observed through post layout simulations that the output and input capacitances (Table 1) of 11T SET static D flip-flop design is less as compared to 12T SET static D flip-flop design. From this point, it is clear that timing delays of the 11T SET static D flip-flop is better than 12T SET static D flip-flop design in terms of setup and hold time (Table 3)

.

4.Conclusion

The simulation results shows that the 11T SET static D flip-flop is better than 12T SET static D flip-flop in terms of area, speed and power consumption and because the one less transistor is used in 11T SET static D flip-flop parasitic capacitances is also less as compared to 12T SET static D flip-flop.

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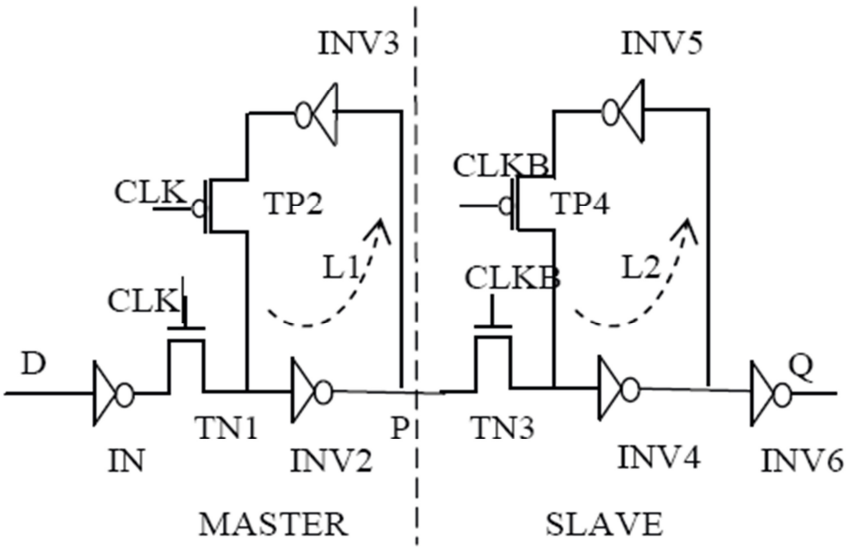

Figure 1: conventional SET static D flip-flop

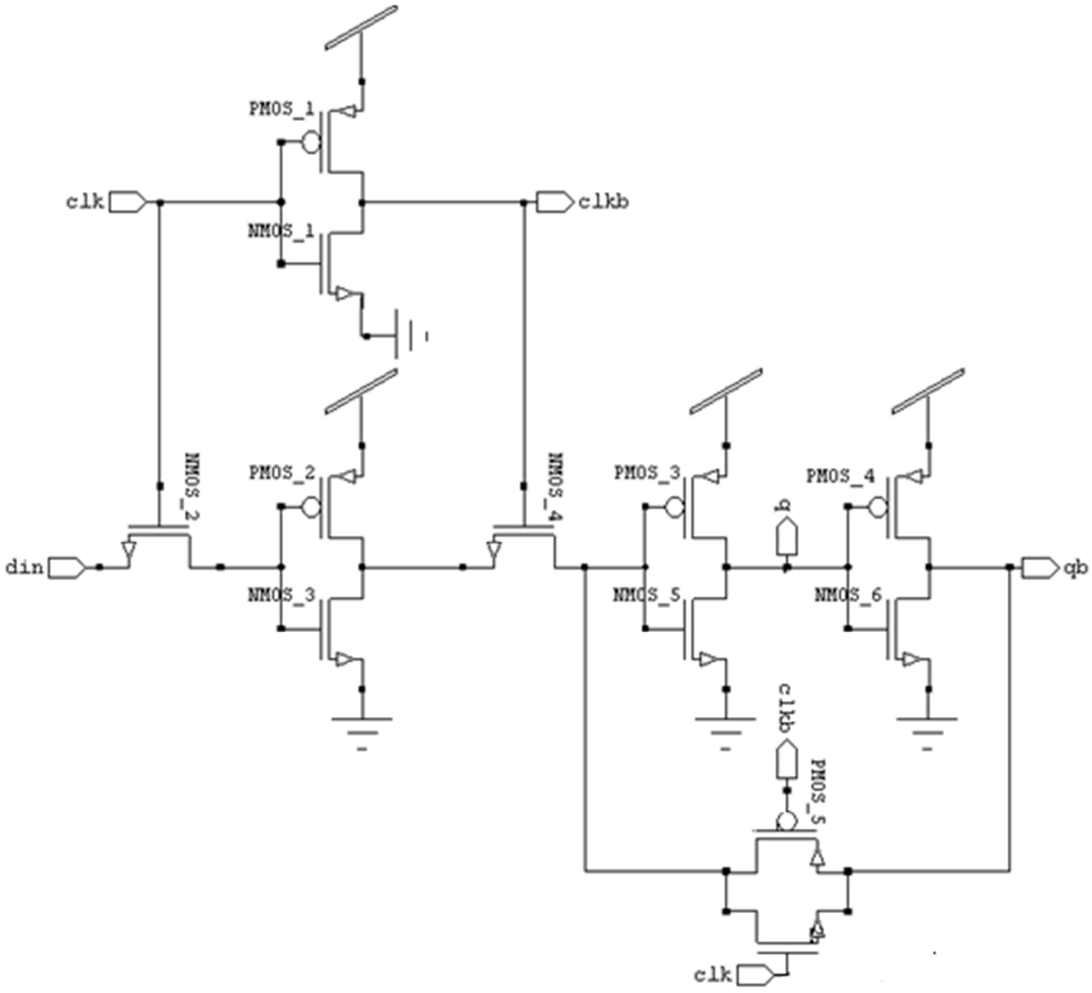

Figure 2: 12T SET static D flip-flop

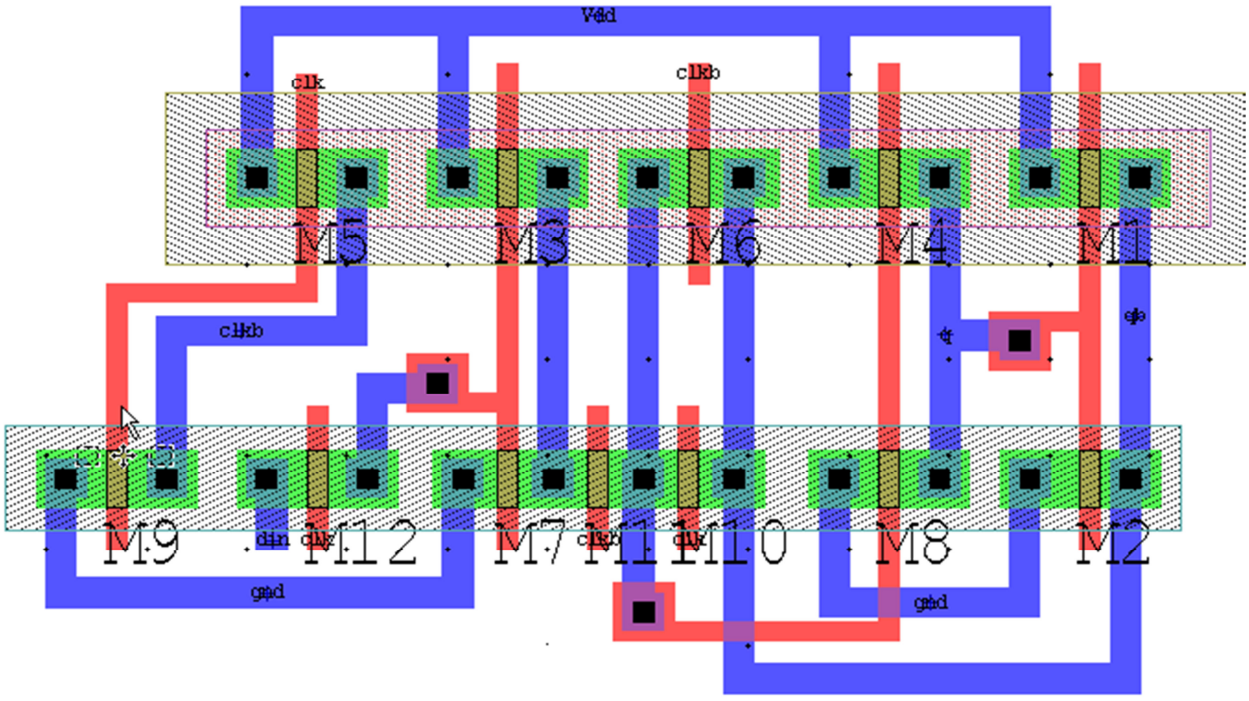

Figure 3: Layout design of 12T SET static D flip-flop

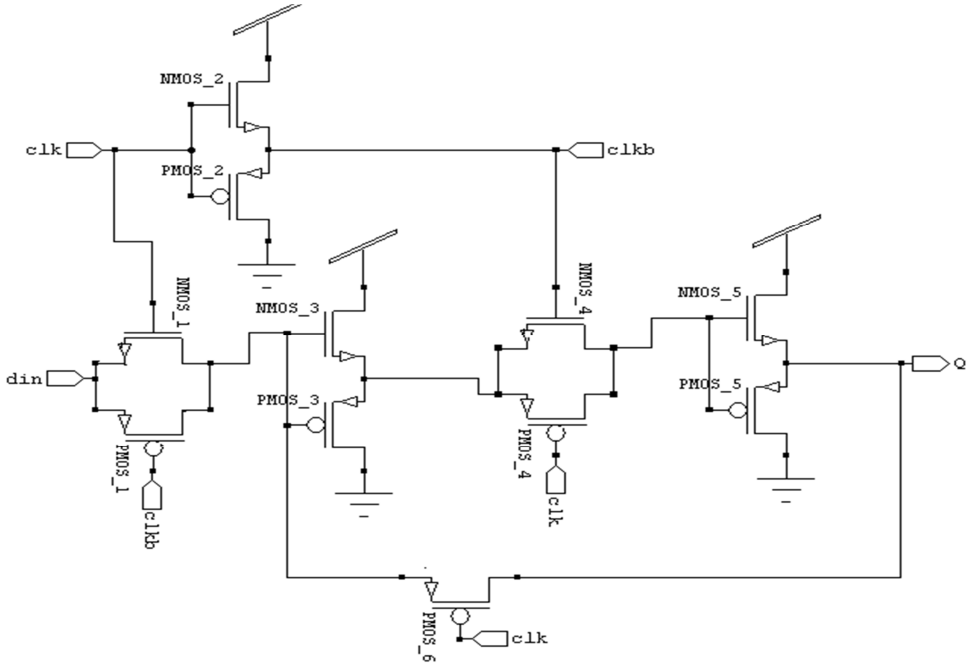

Figure 4: 11T SET static D flip-flop

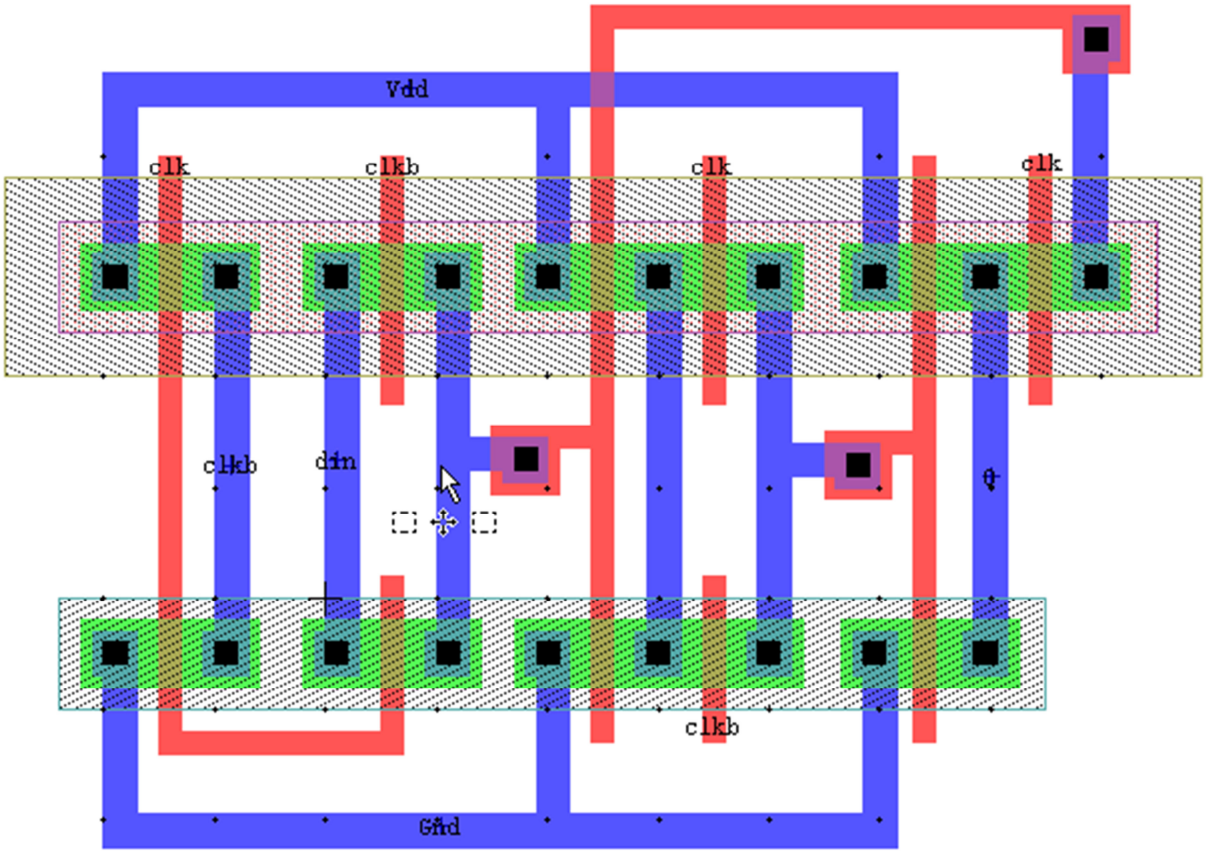

Figure 5: Layout design of 11T SET static D flip-flop

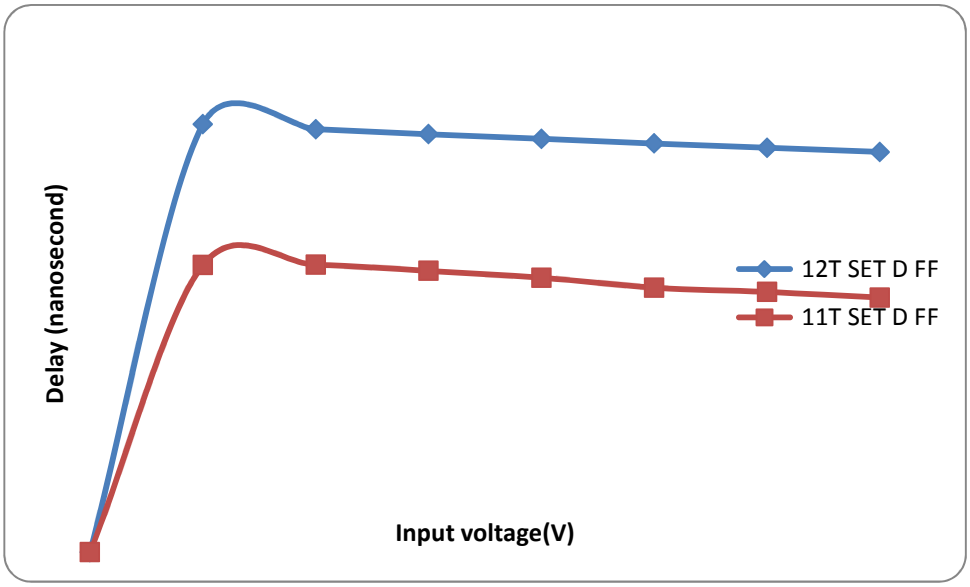

Figure 6. Delay at various input voltage in 65nm Technology

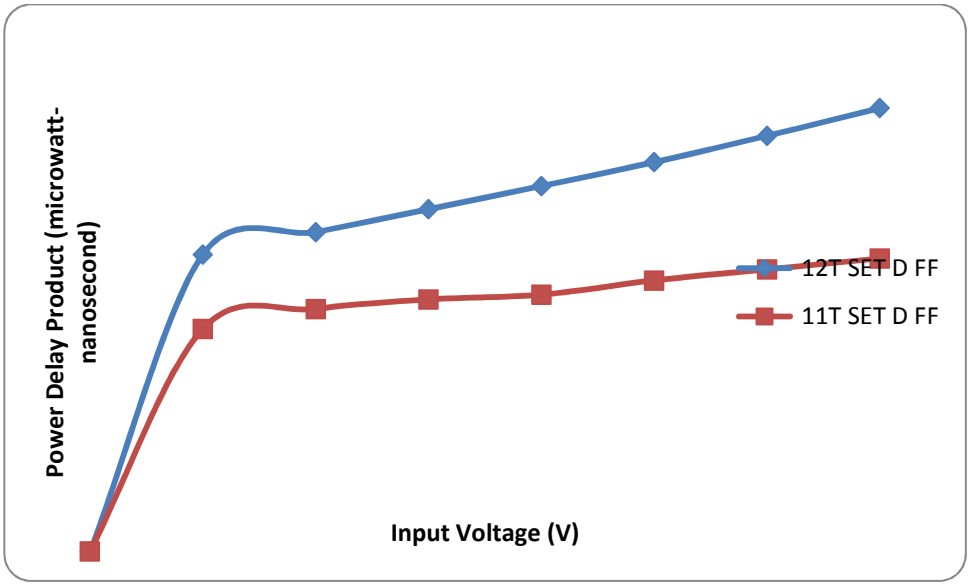

Figure 7. Power Delay Product at various input voltage in 65nm Technology

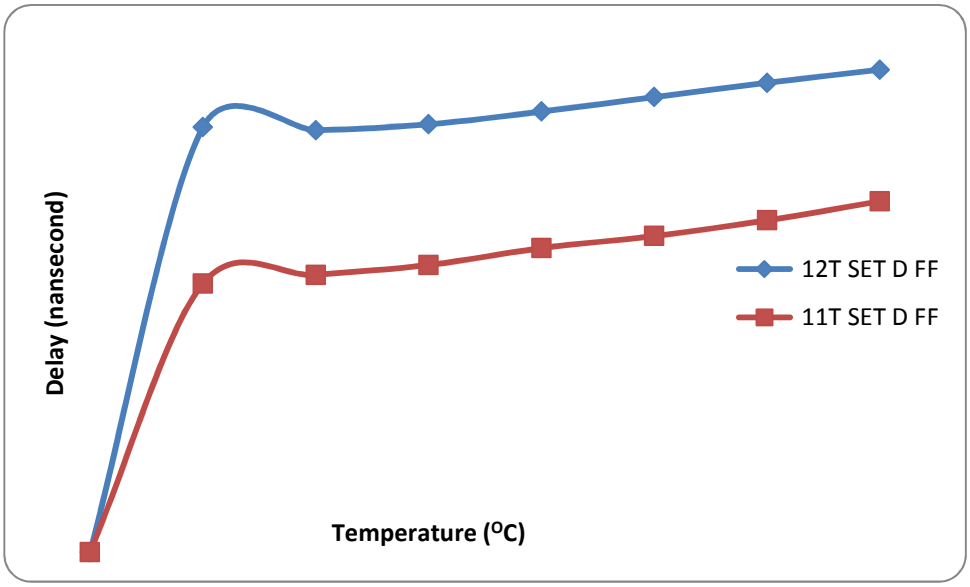

Figure 8. Delay at various temperature in 65nm Technology

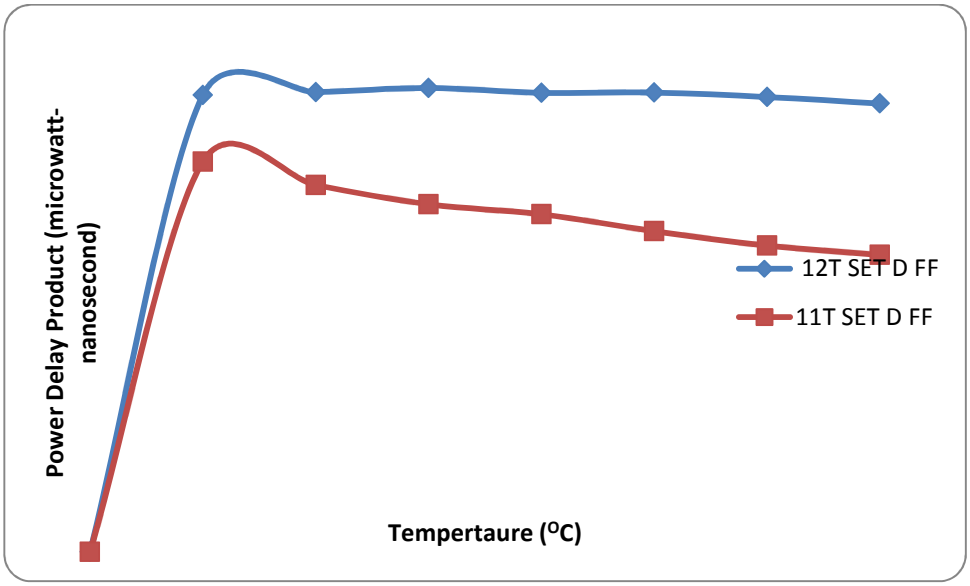

Figure 9. Power Delay Product at temperature voltage in 65nm Technology

Table 1. Input and Output capacitances of SET D flip-flop

	12T SET D Flip-Flop	11T SET D Flip-Flop
Input Capacitance(Ff)	2.1400	5.1354
Output Capacitance (Ff)	12.540	5.5304

Table 2. Setup and Hold Time of SET D flip-flop

	12T SET D Flip-Flop	11T SET D Flip-Flop
Setup time (ns)	112.910	54.157
Hold time (ns)	0.0329	0.0141

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